

FIG. 2

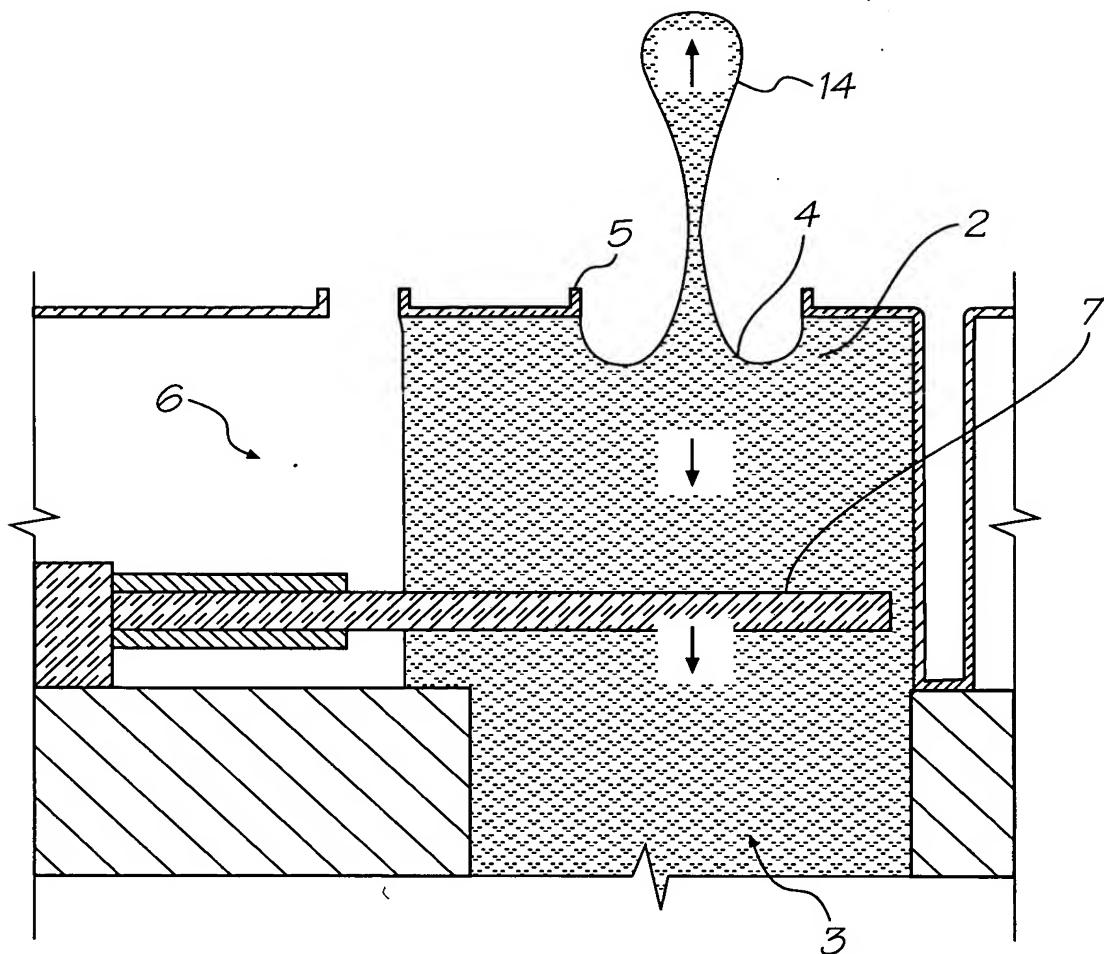


FIG. 3

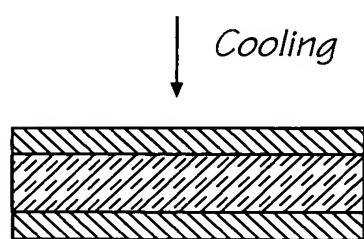
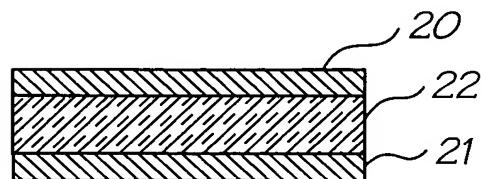


FIG. 4



FIG. 5

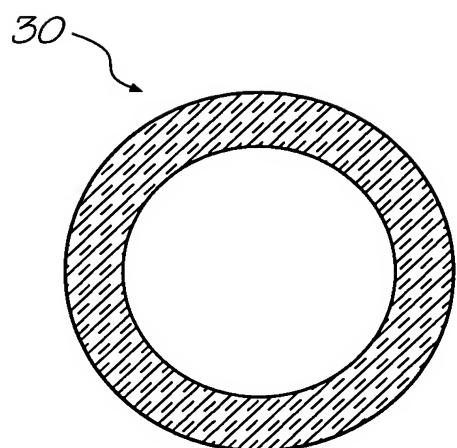


FIG. 6

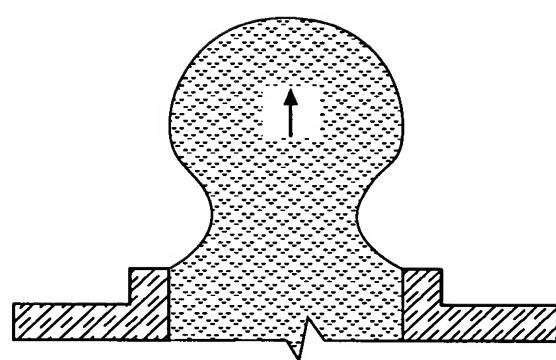


FIG. 7

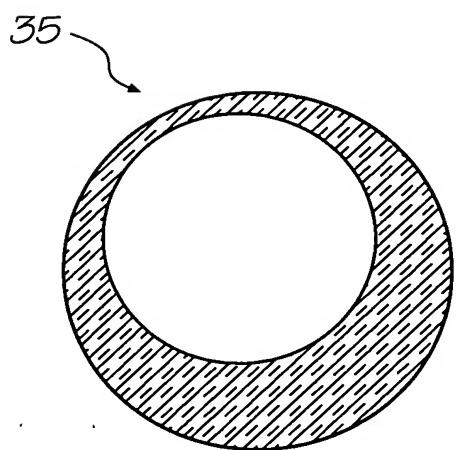


FIG. 8

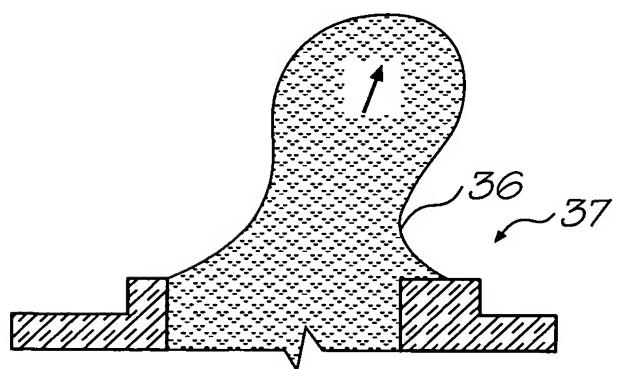


FIG. 9

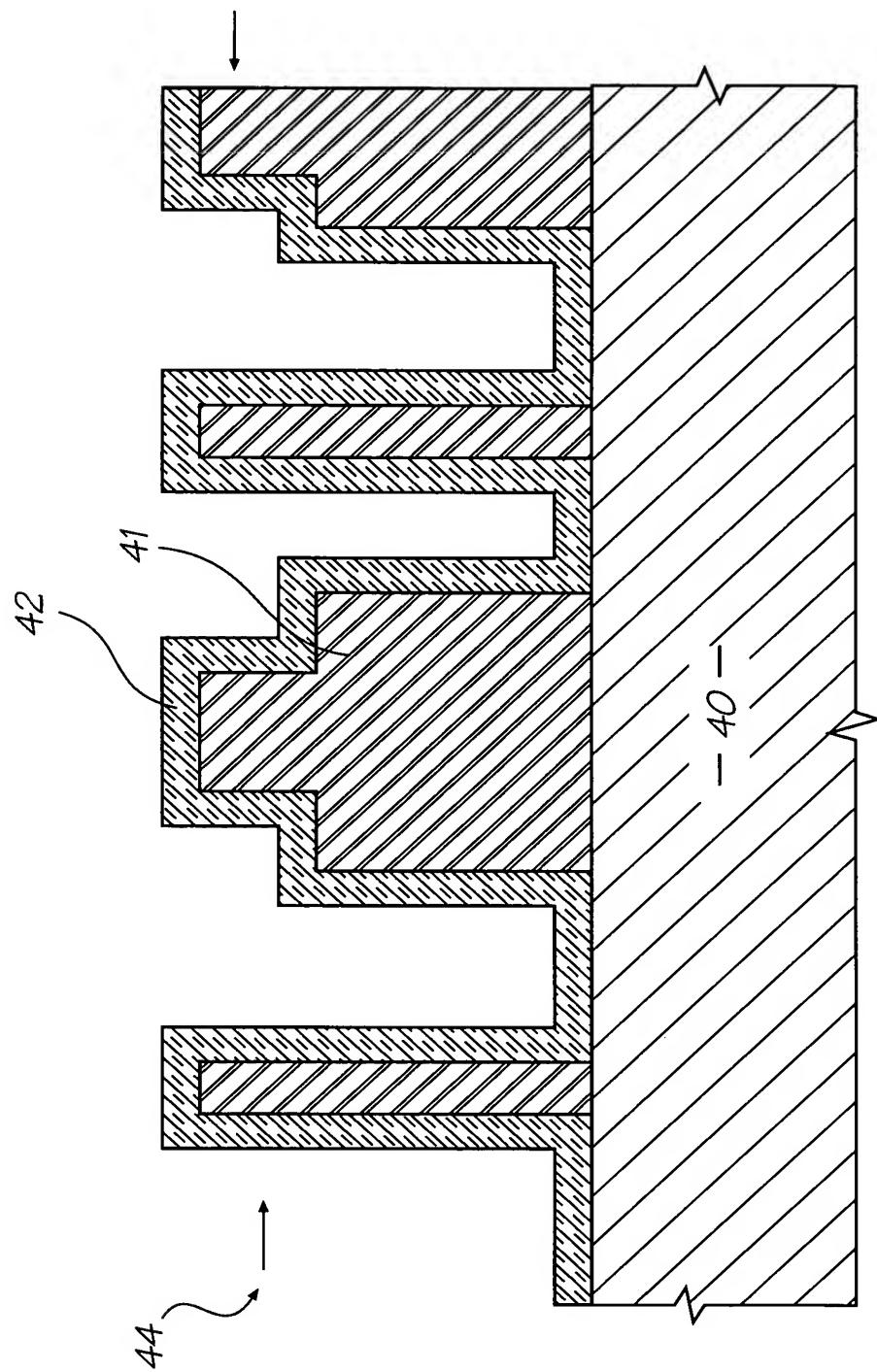


FIG. 10

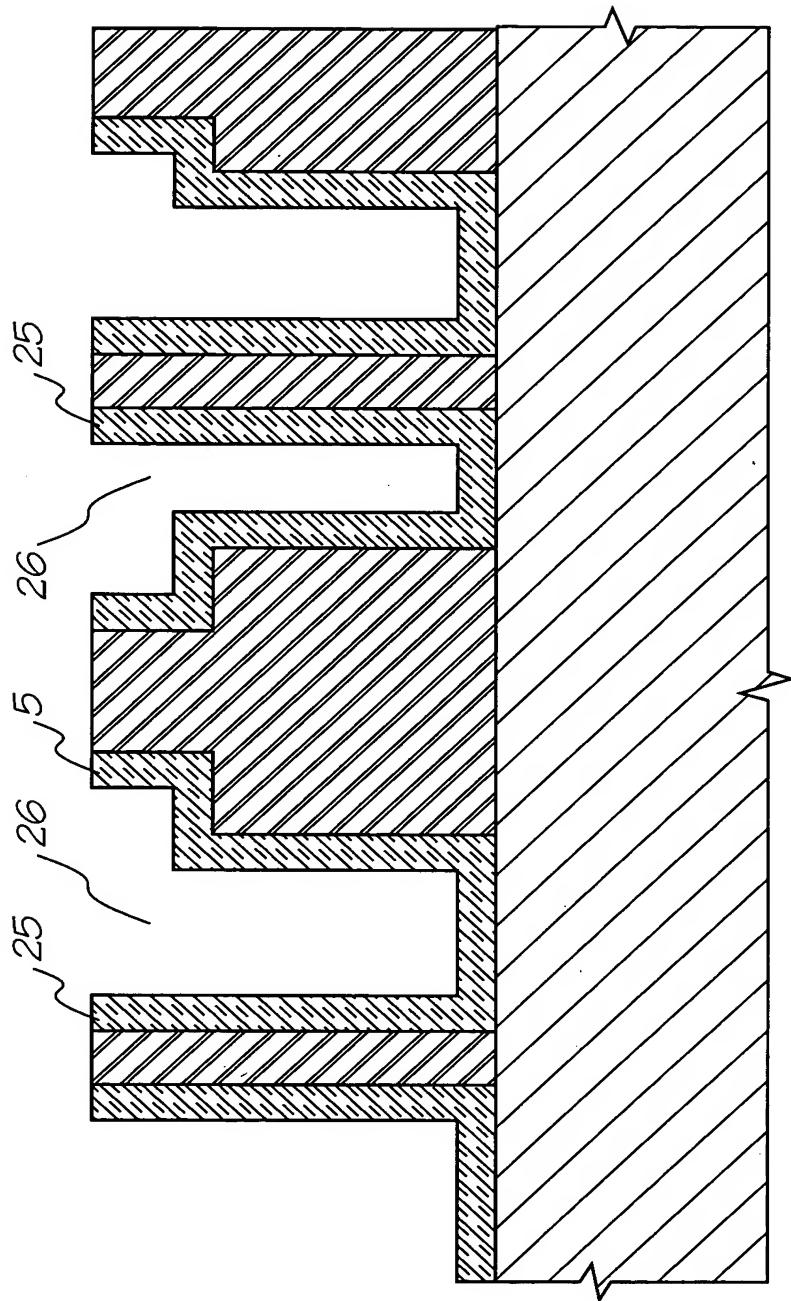


FIG. 11

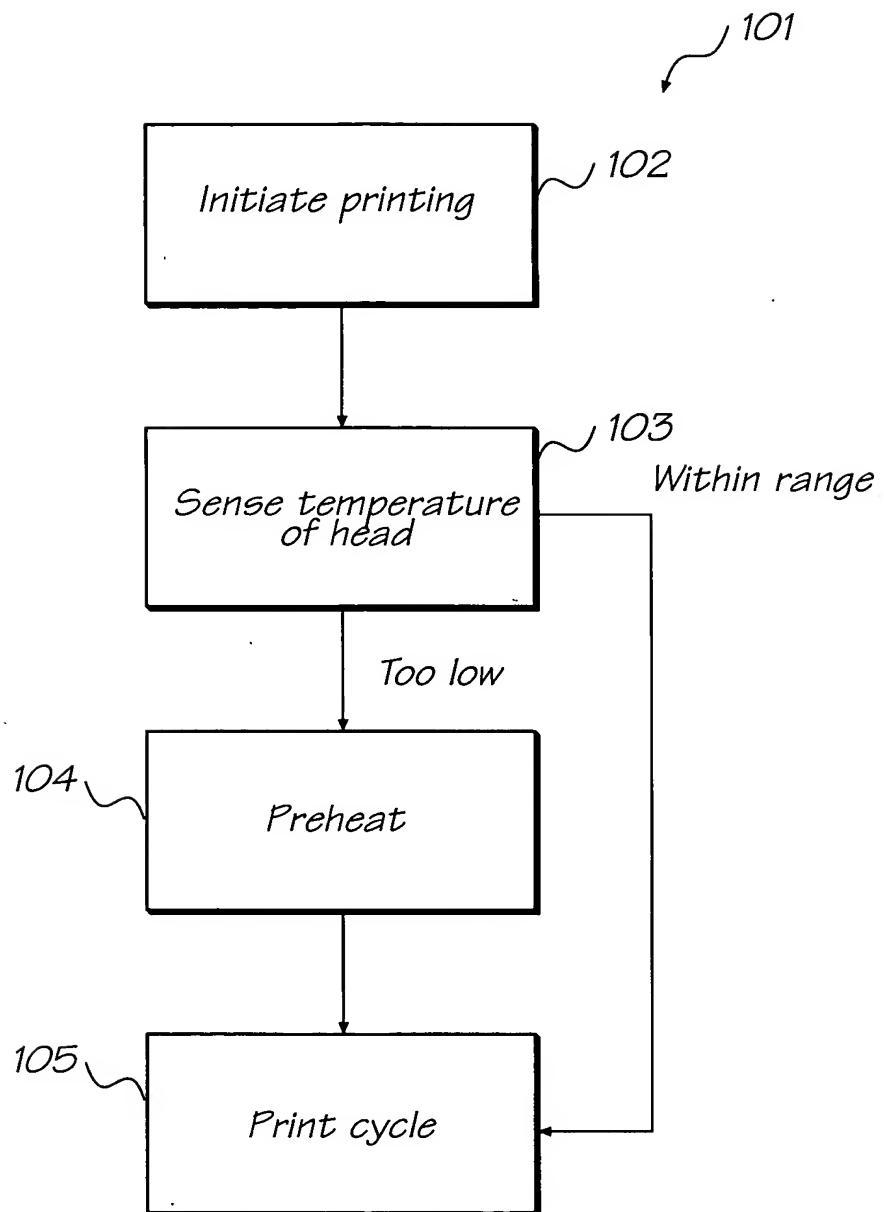


FIG. 12

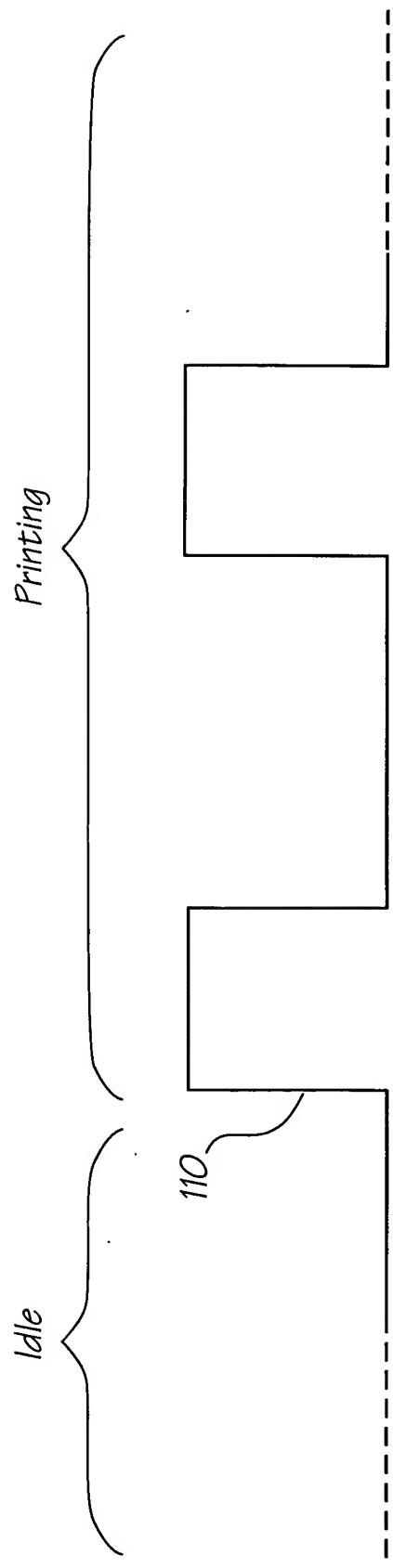


FIG. 13

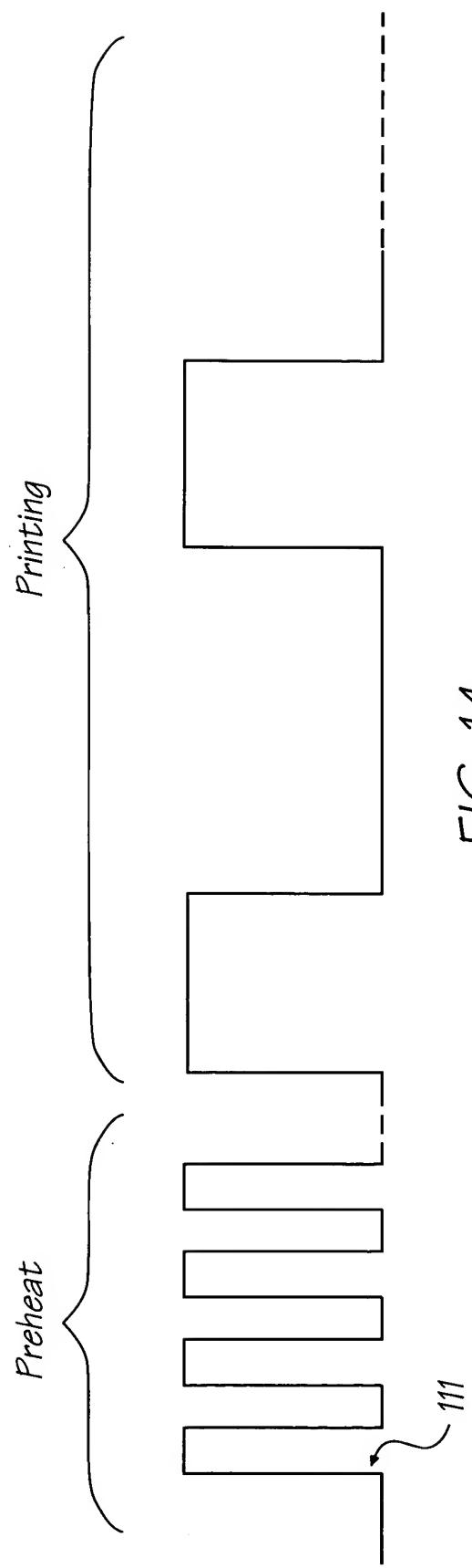


FIG. 14

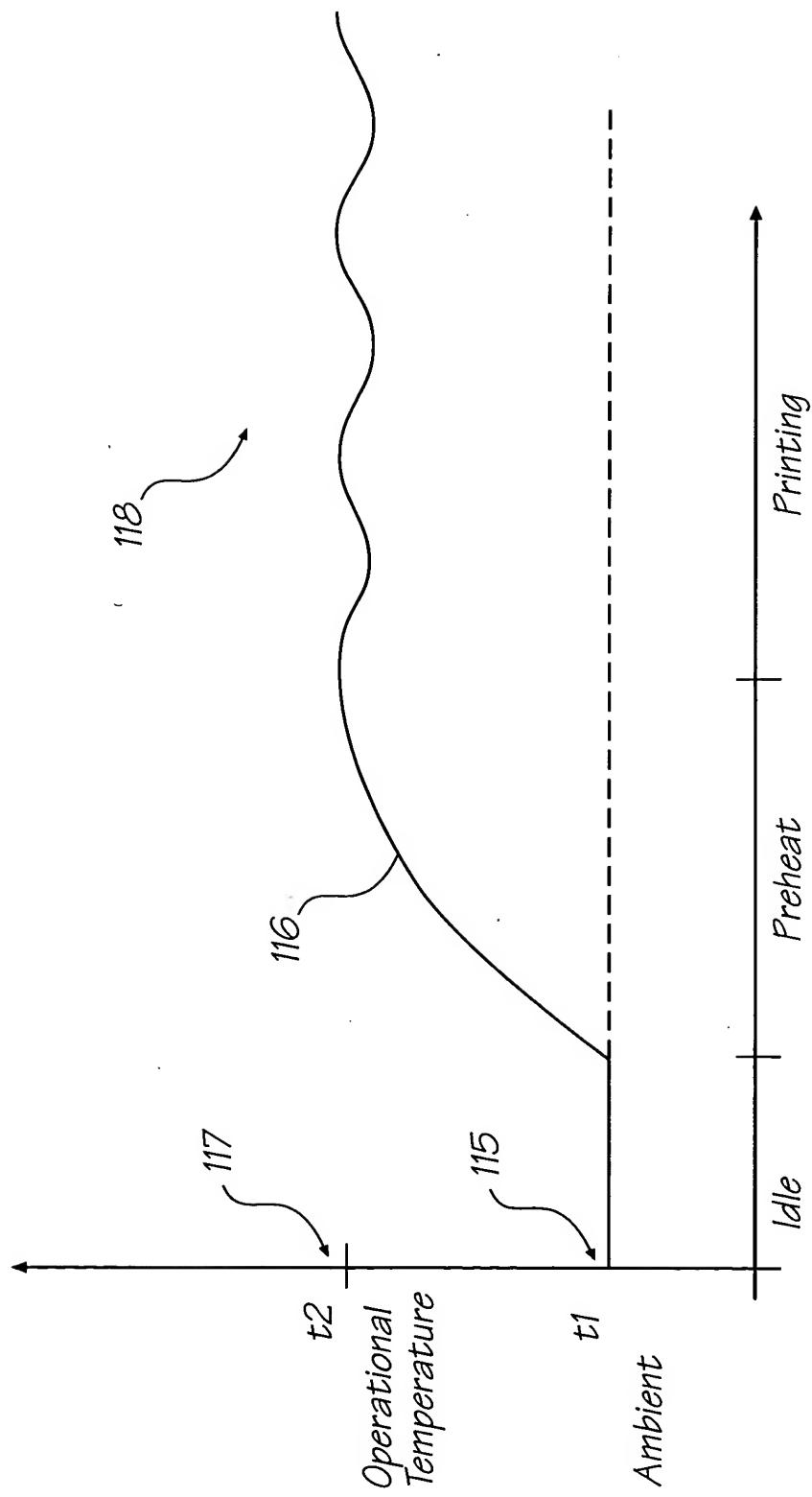


FIG. 15

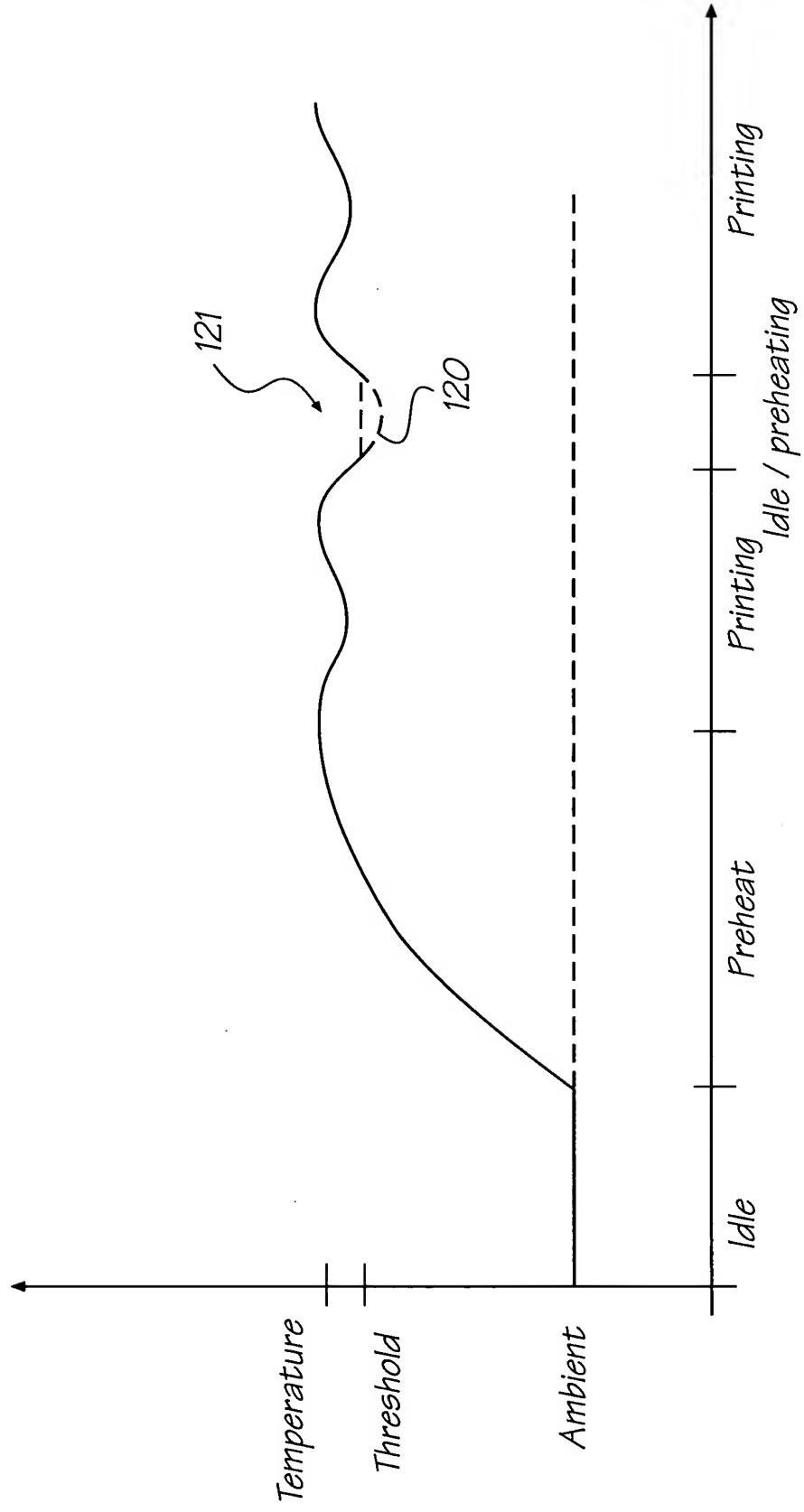


FIG. 16

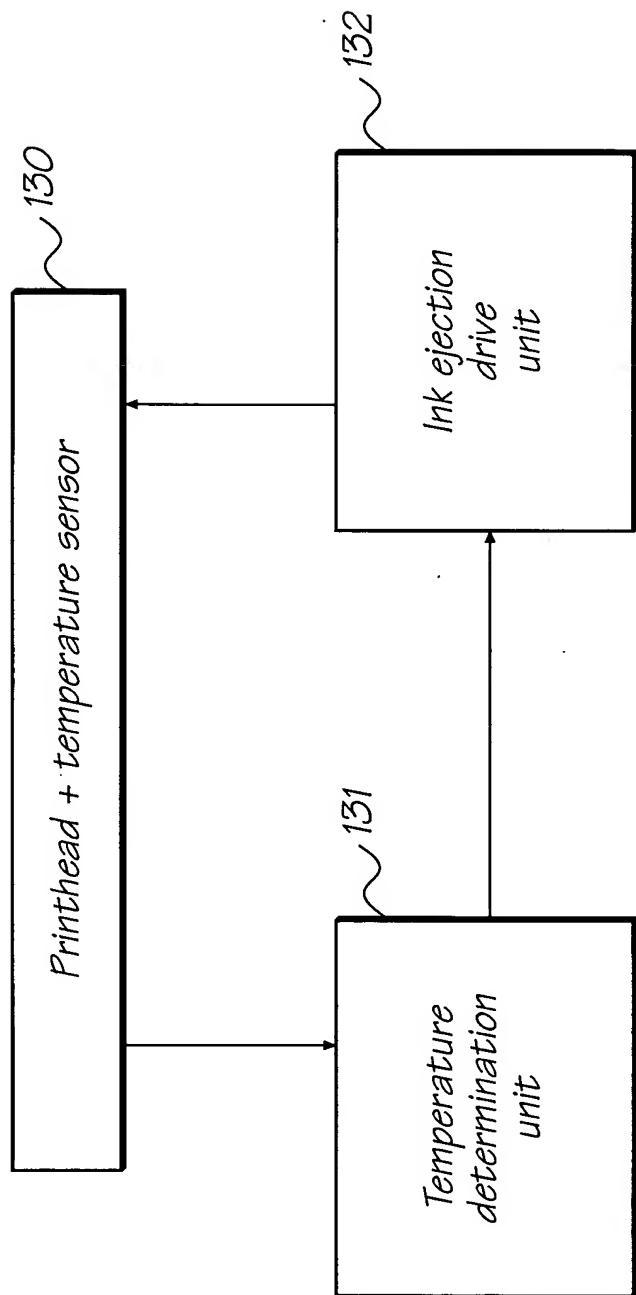


FIG. 17

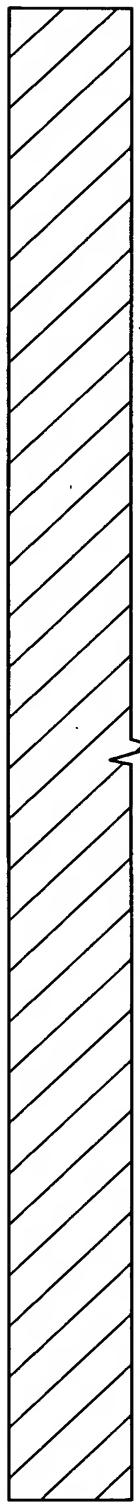


FIG. 18

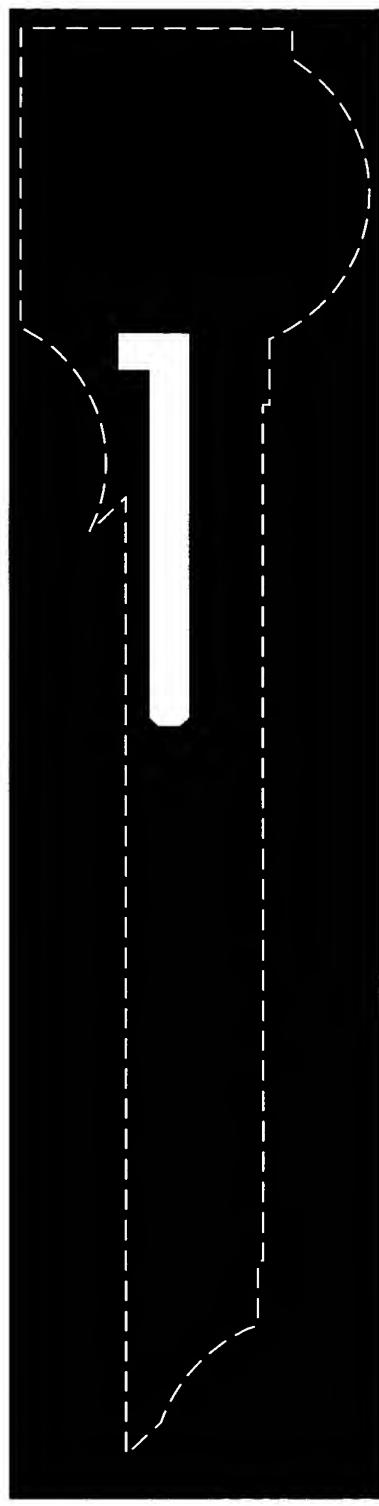
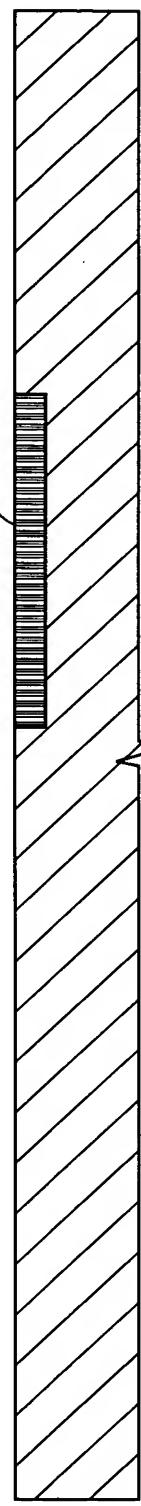


FIG. 19

N-Well mask



Implant N-Well

FIG. 20

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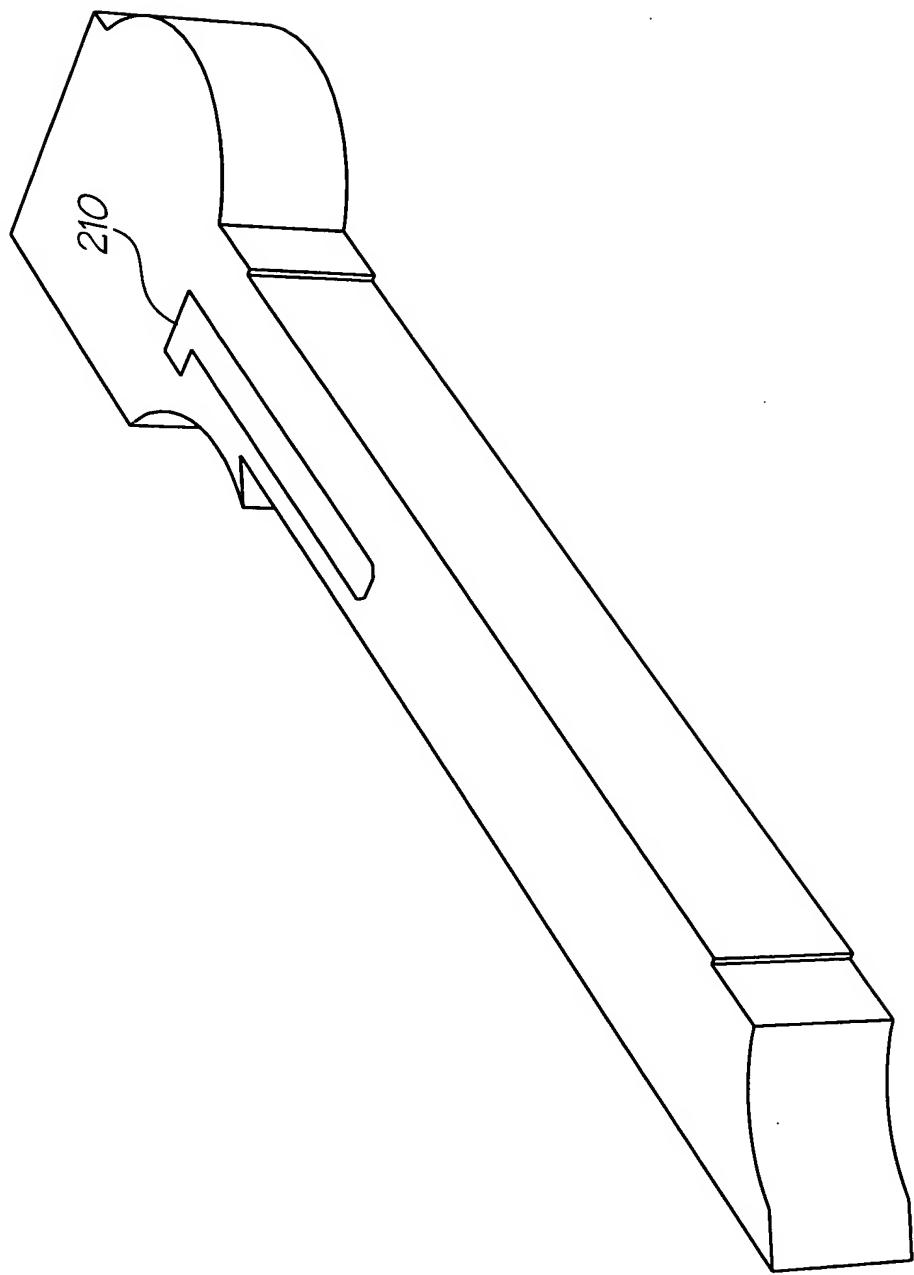
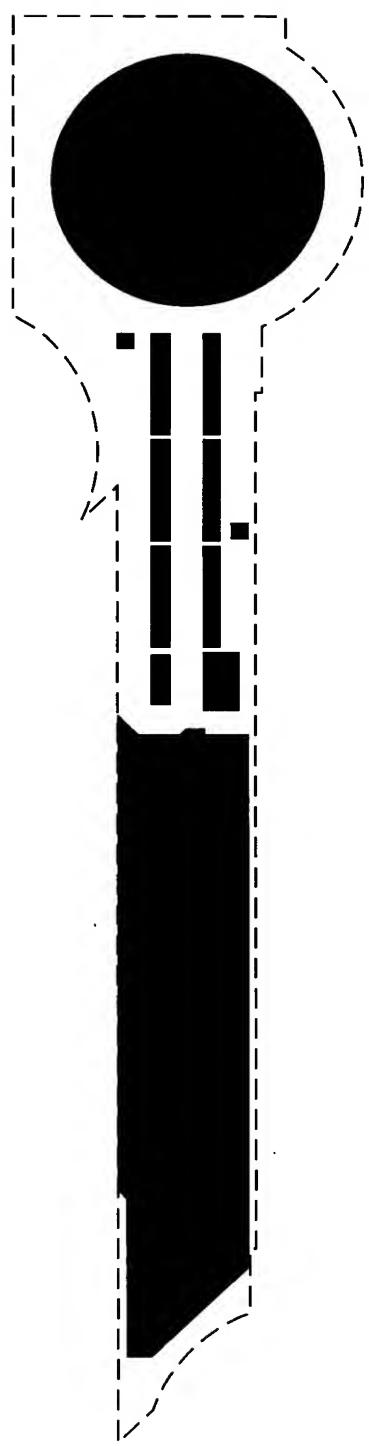
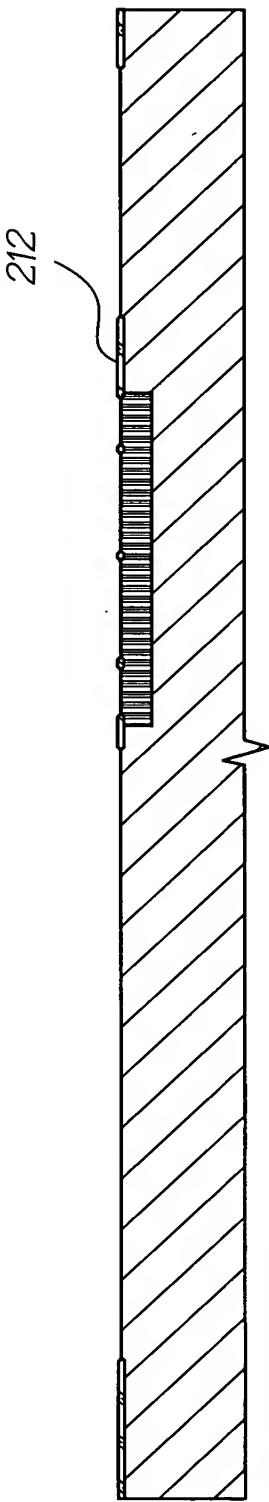


FIG. 21



*Active mask*

*FIG. 22*



*Grow field oxide*

*FIG. 23*

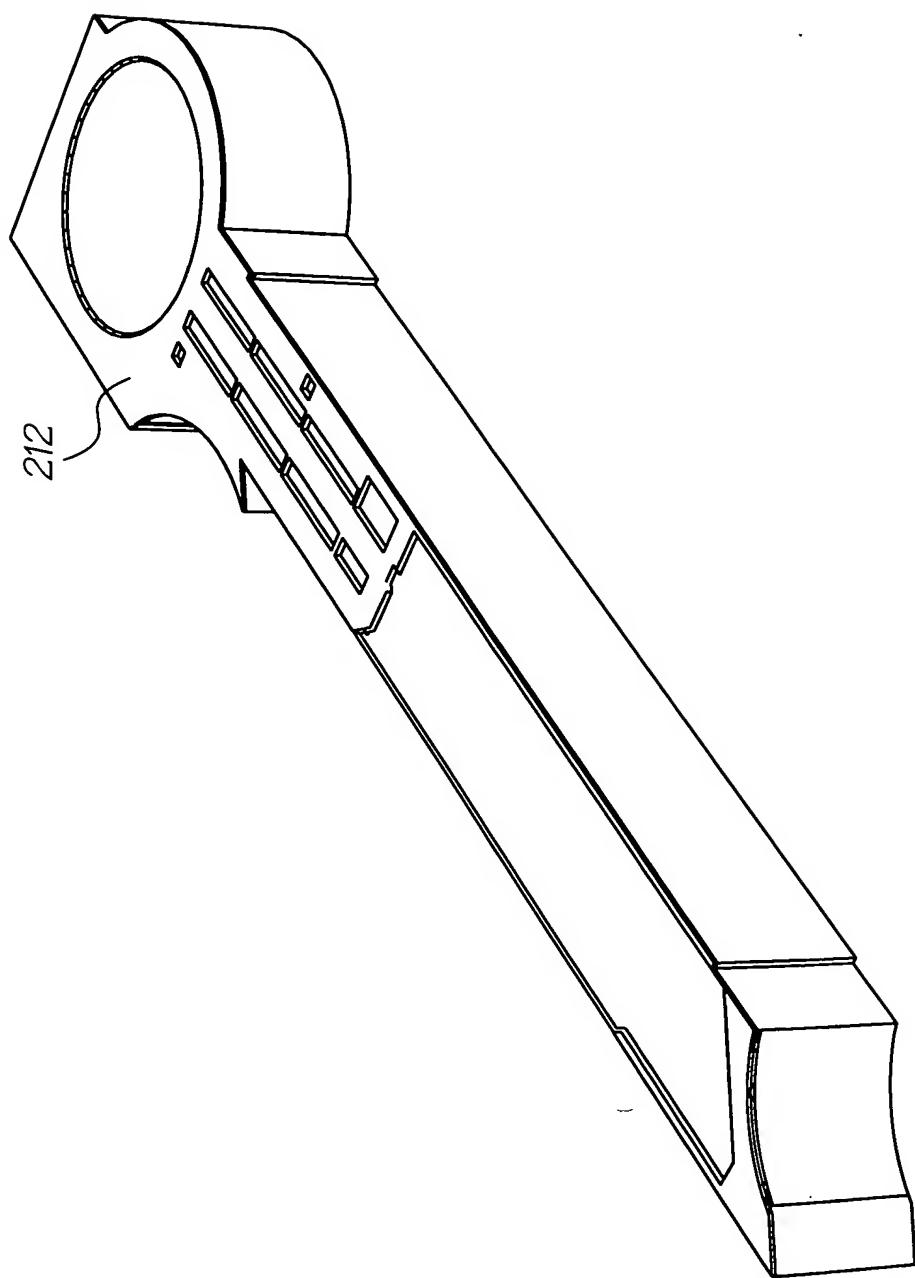
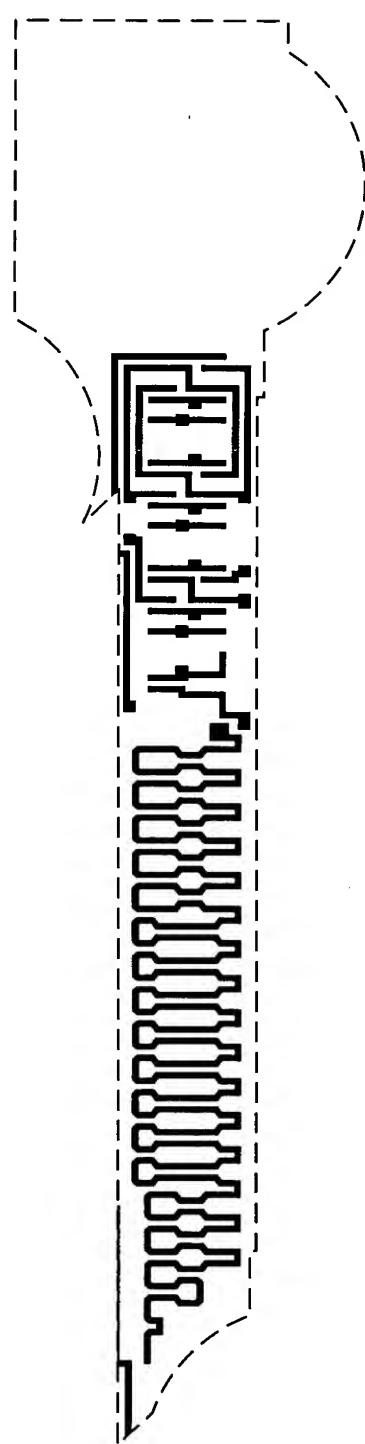
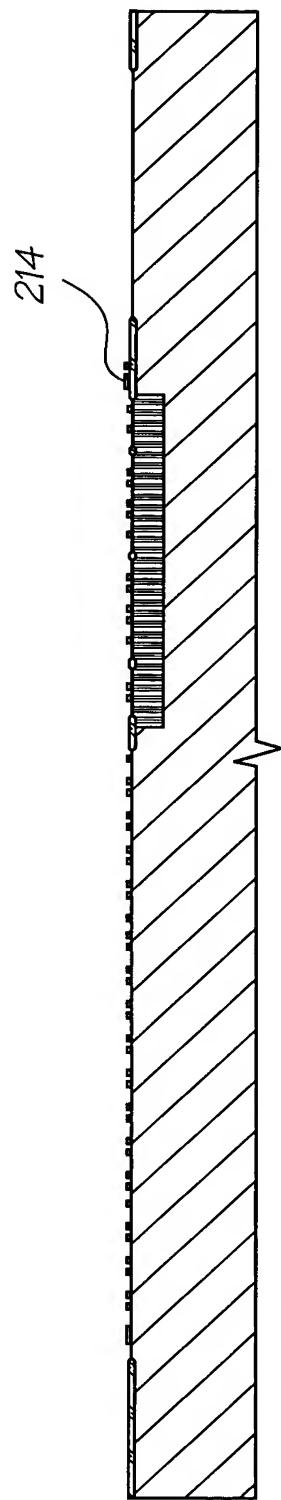


FIG. 24



Poly mask

FIG. 25



Deposit poly

FIG. 26

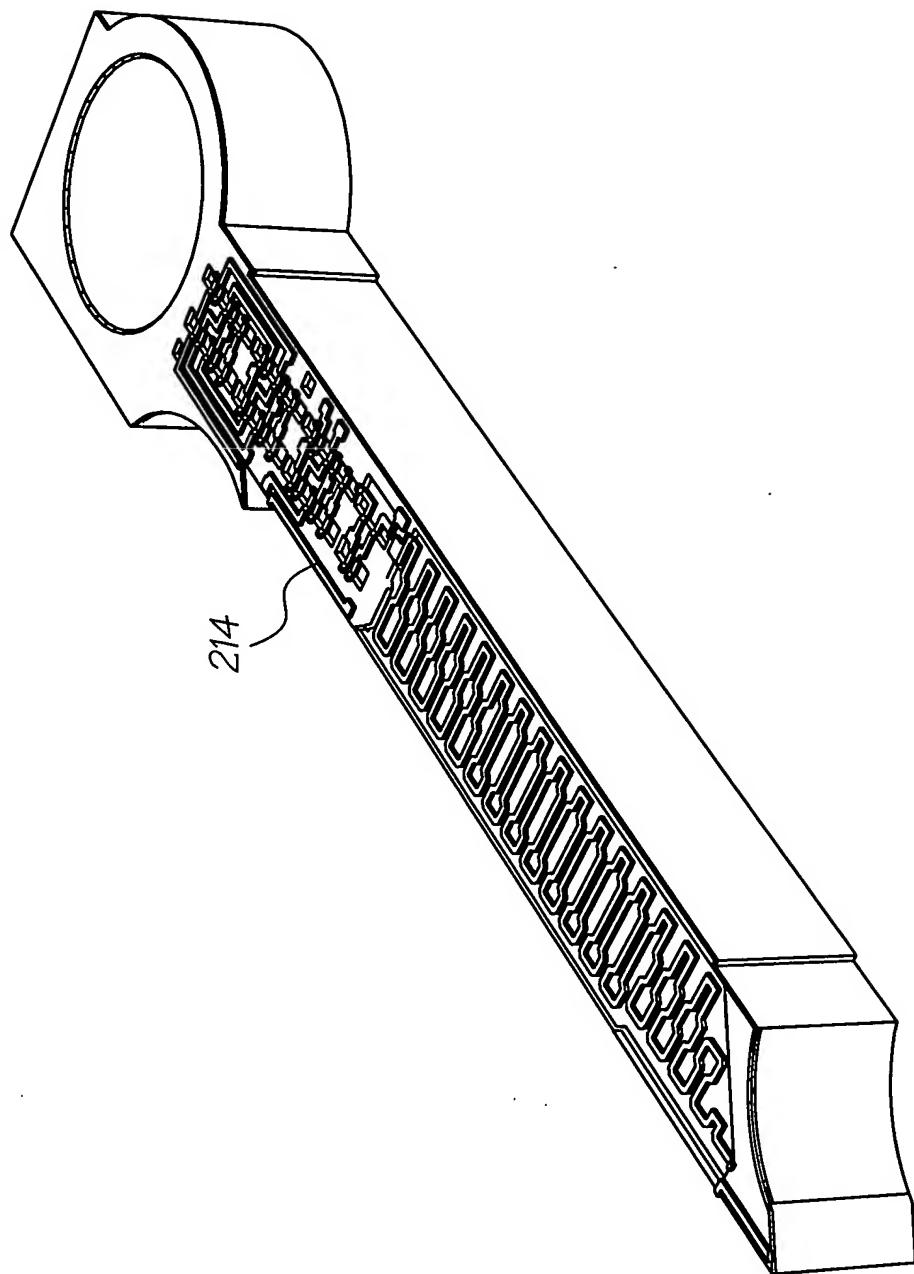


FIG. 27

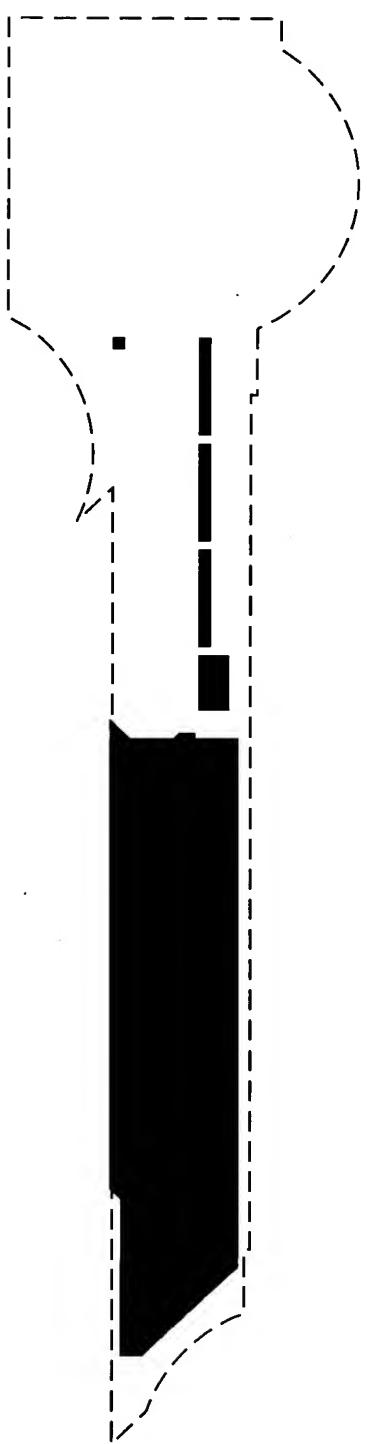


FIG. 28

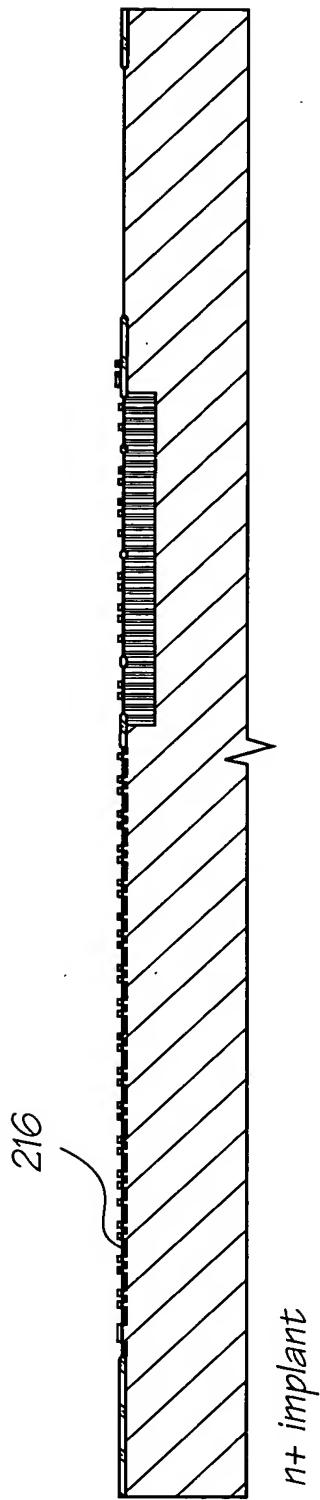


FIG. 29

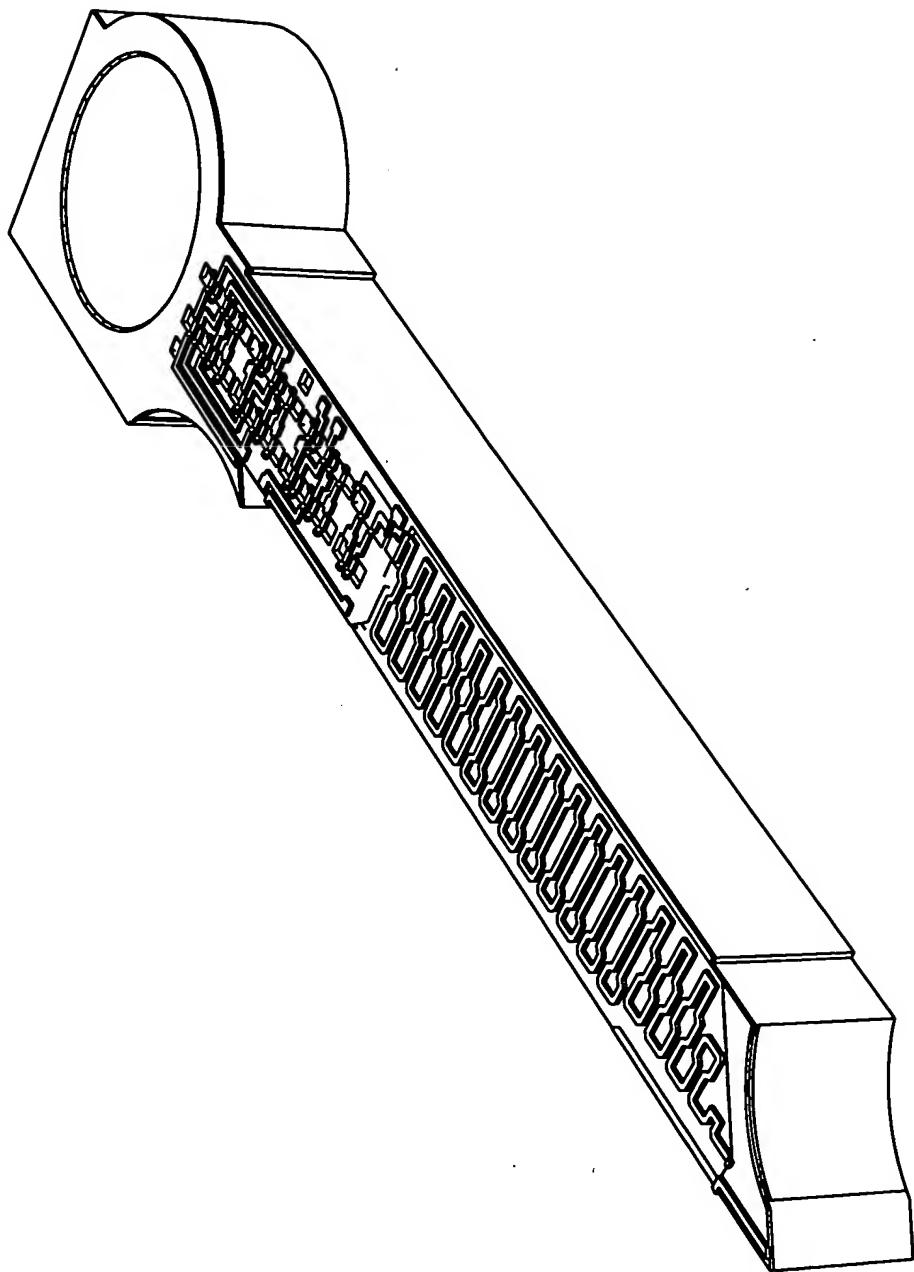


FIG. 30

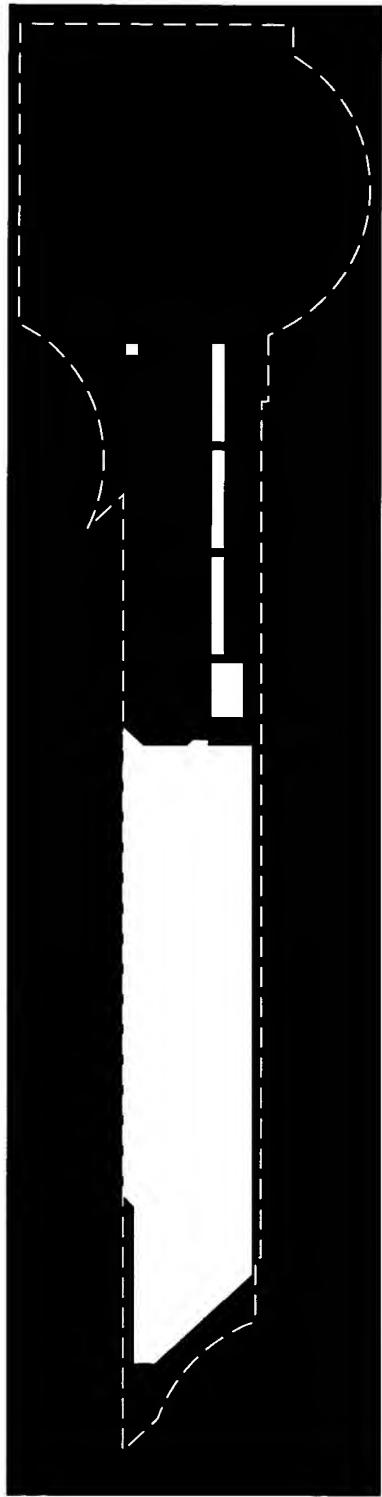


FIG. 31  
 $p^+$  mask

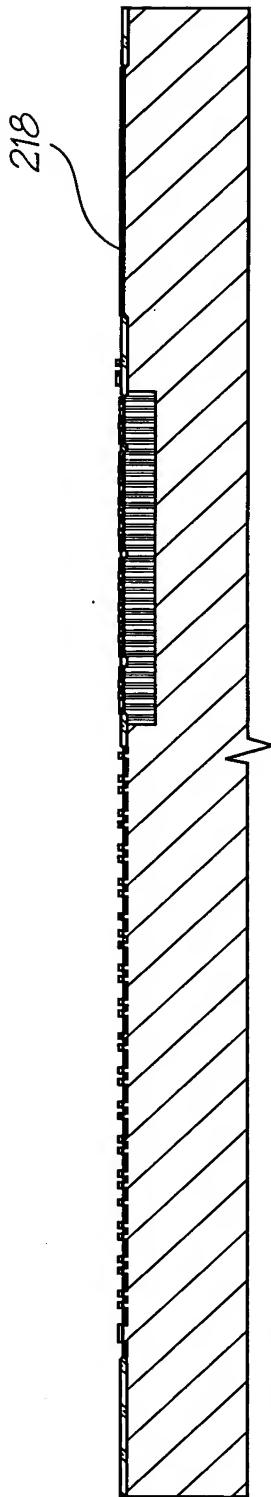


FIG. 32  
 $p^+$  implant

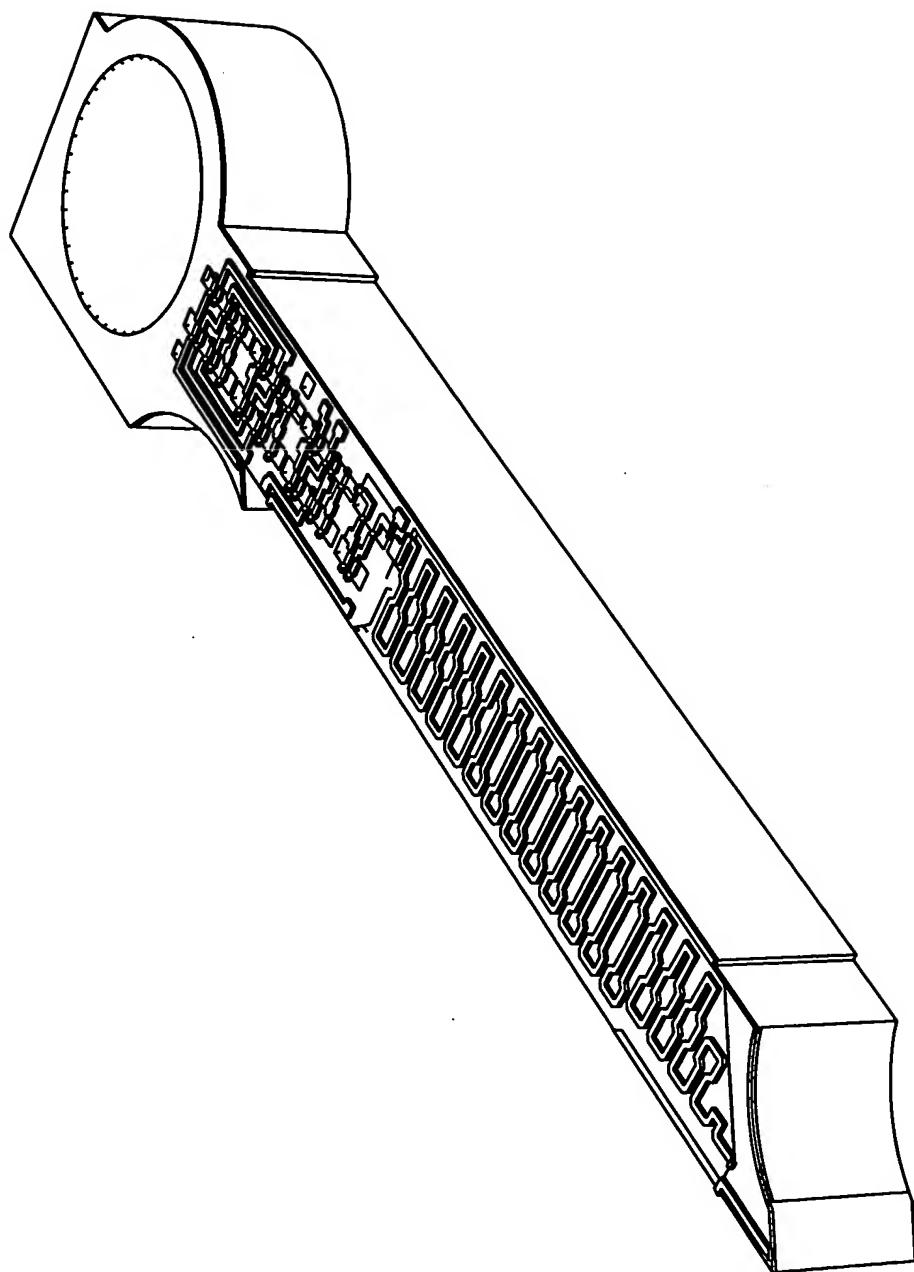


FIG. 33

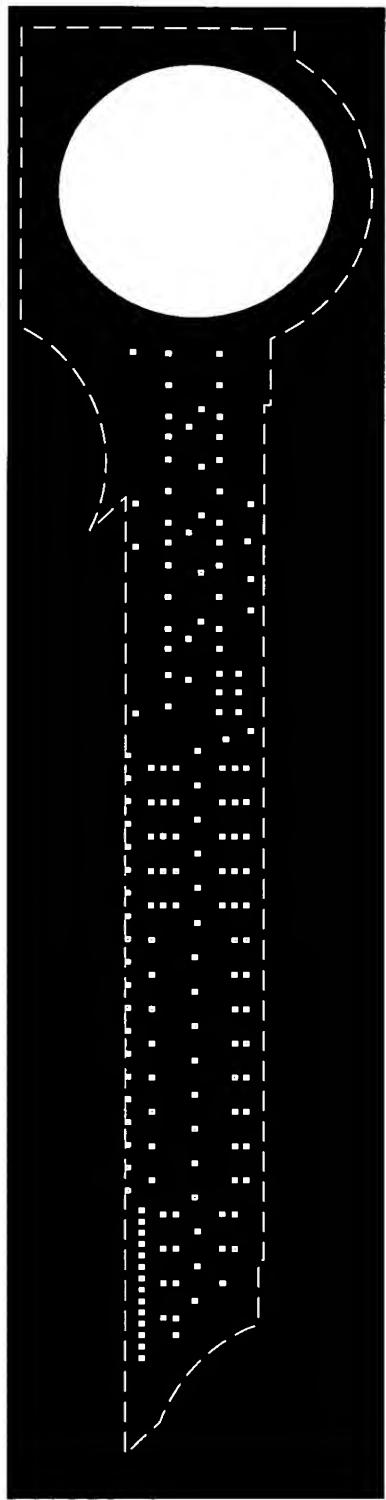


FIG. 34

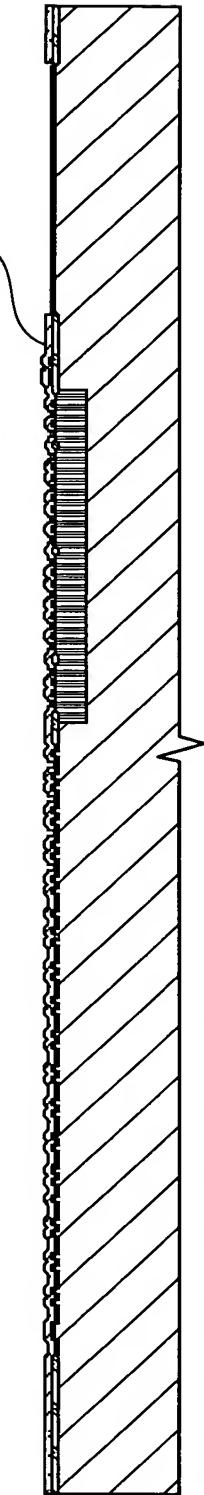


FIG. 35

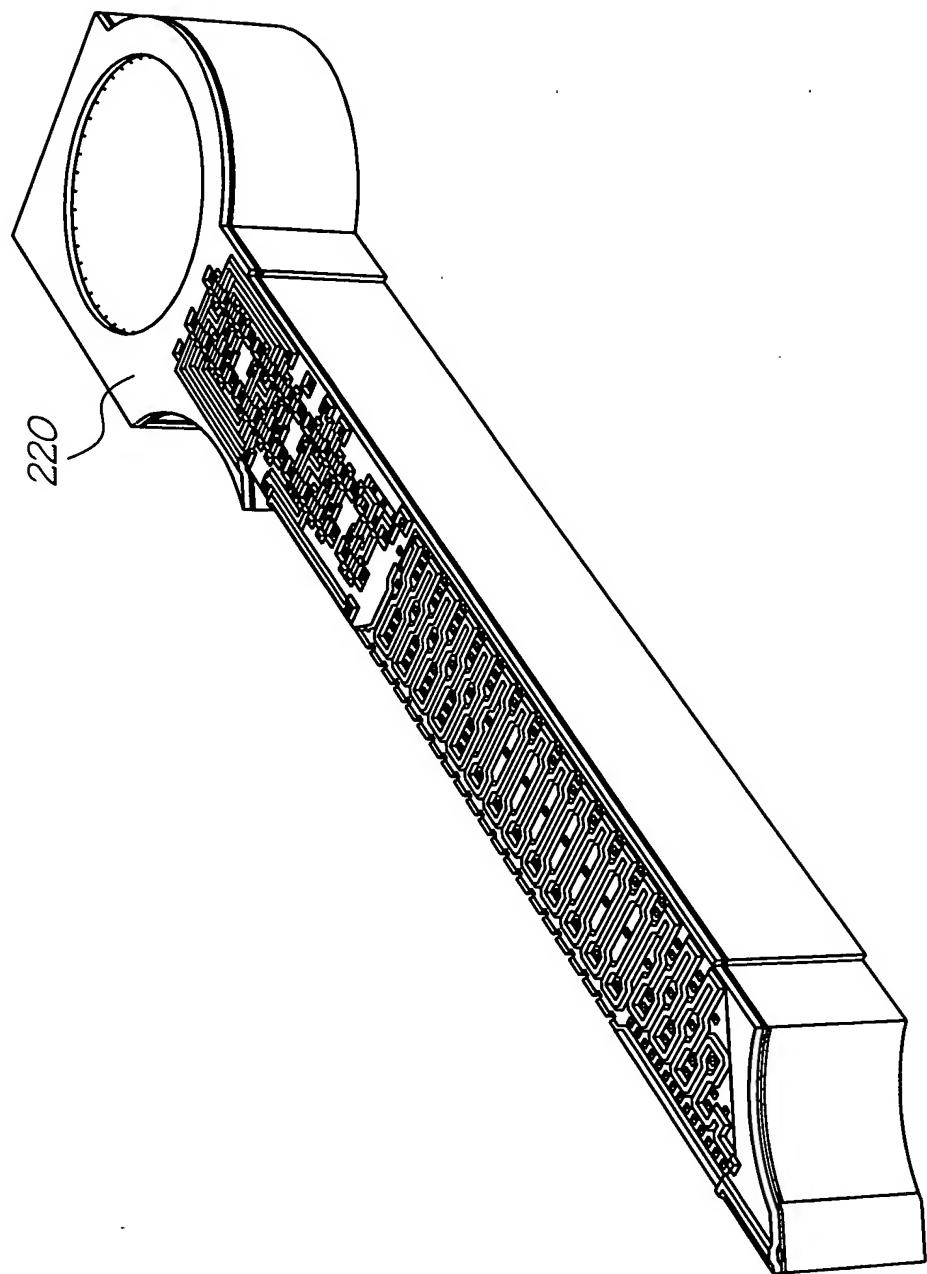
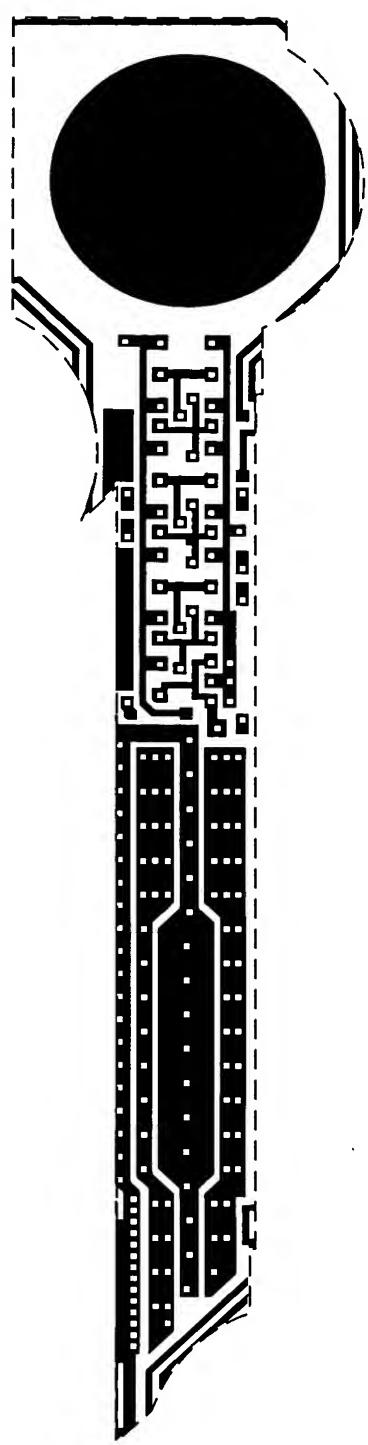
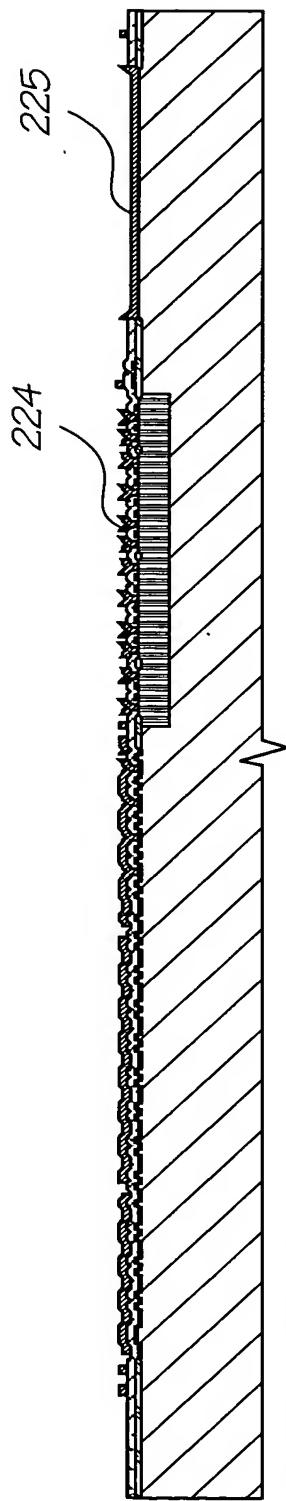


FIG. 36



Metal 1 mask

FIG. 37



Deposit Metal 1

FIG. 38

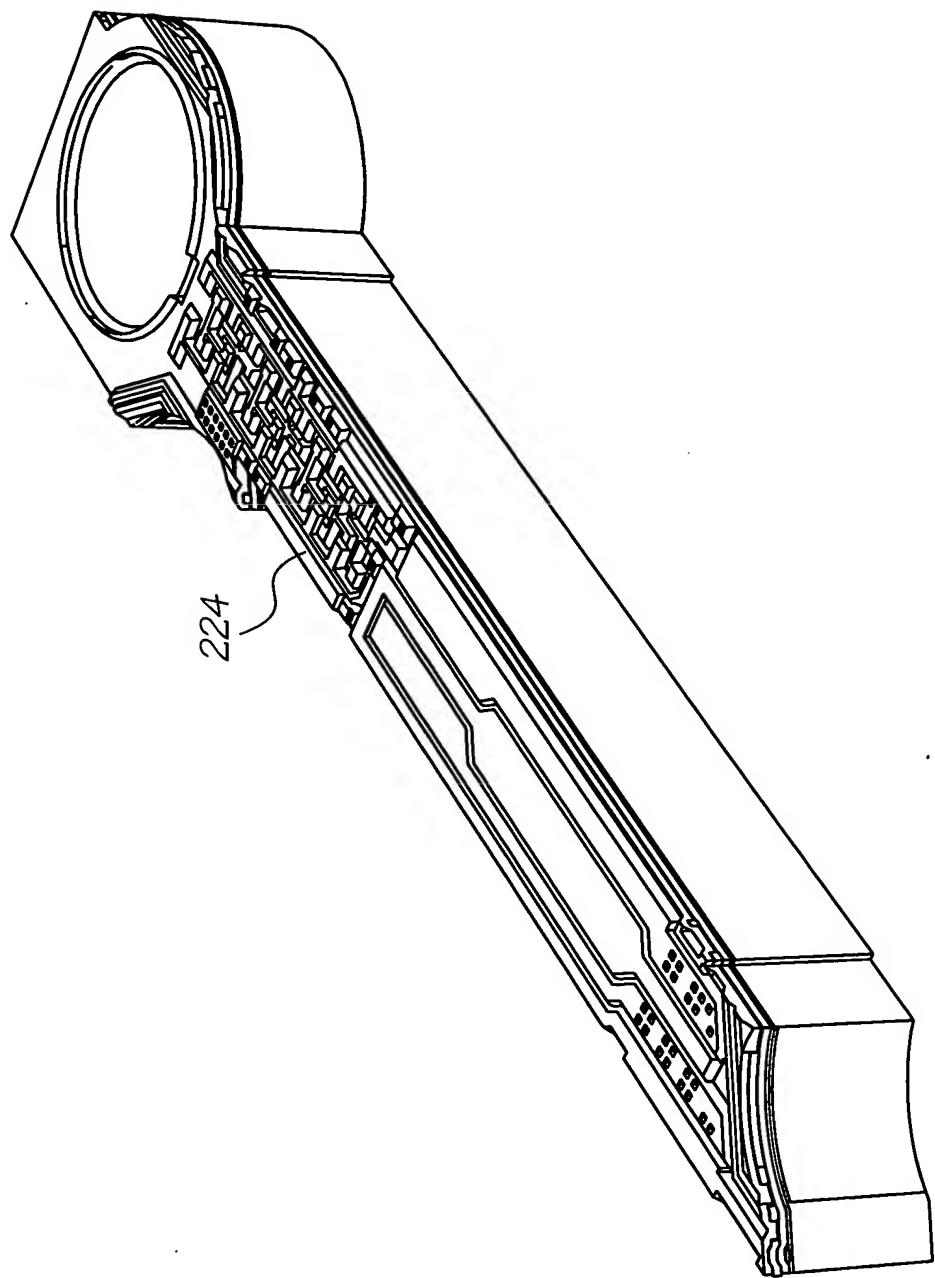
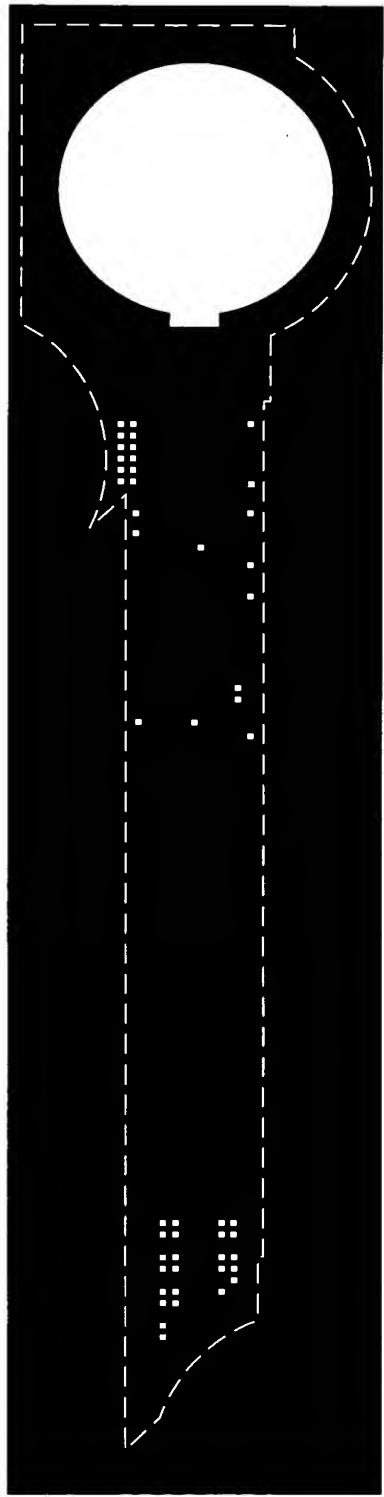
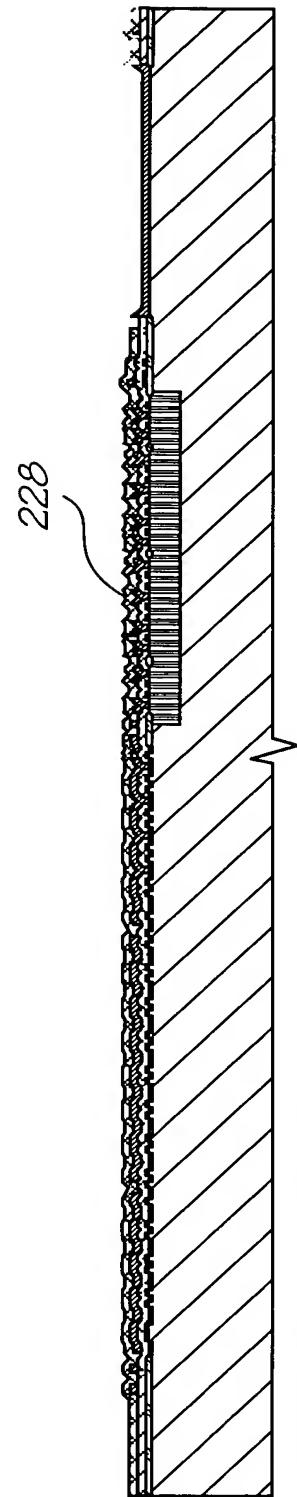


FIG. 39



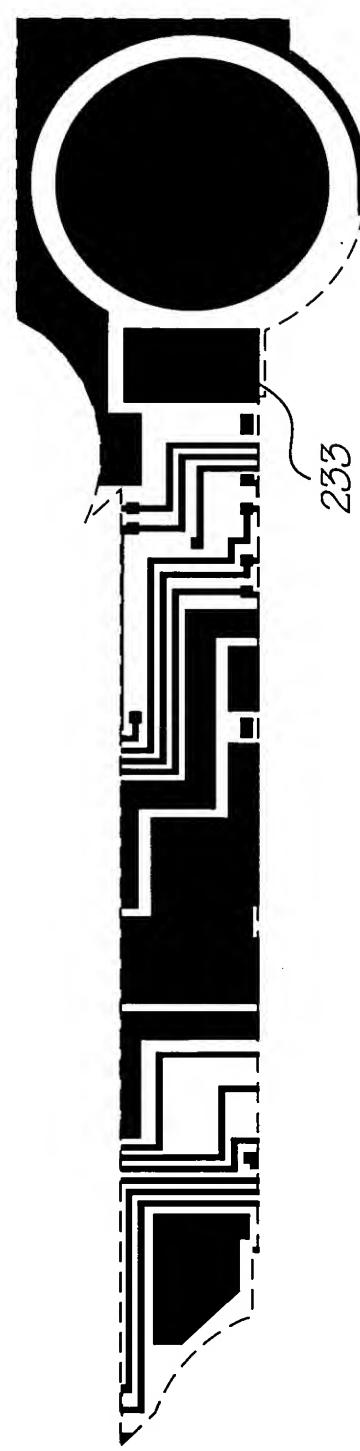
Via 1 mask

FIG. 40



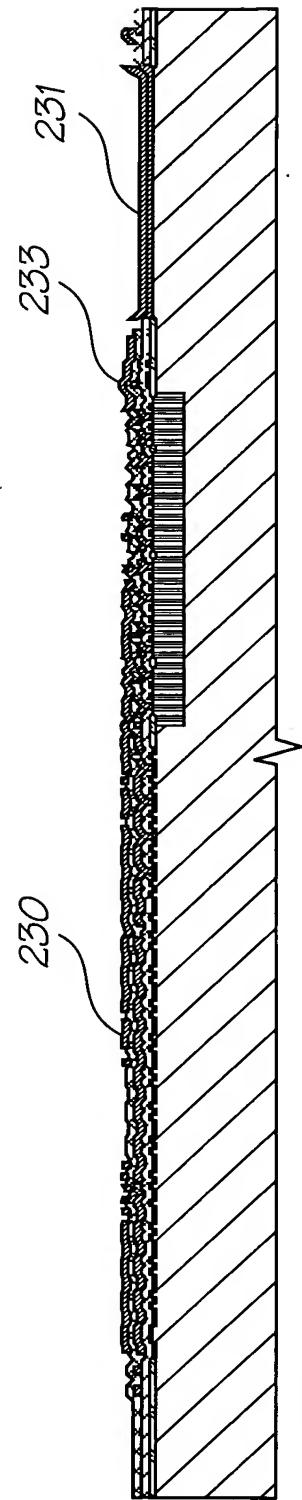
Deposit ILD 2, etch vias

FIG. 41



Metal 2 mask

FIG. 42



Deposit metal 2

FIG. 43

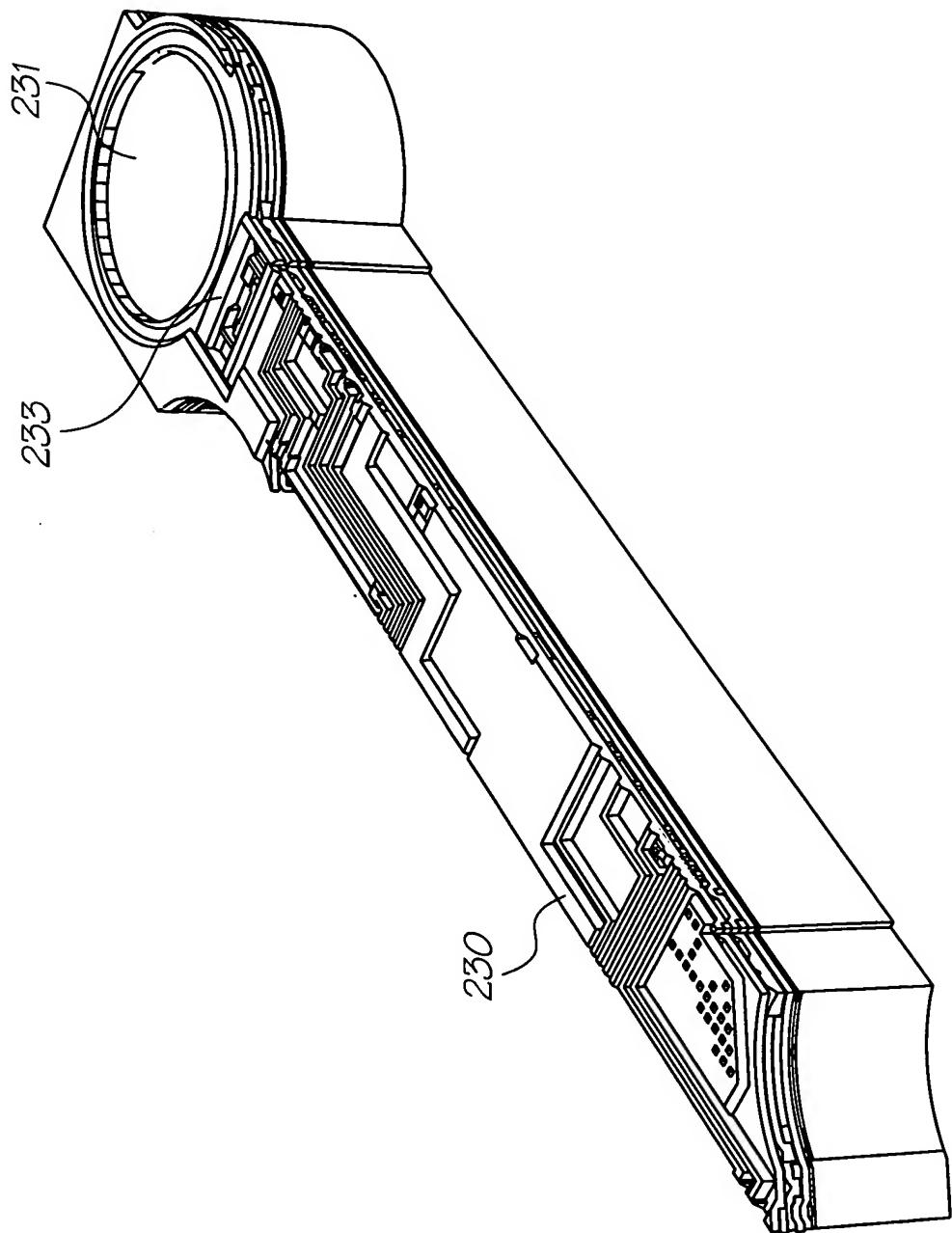
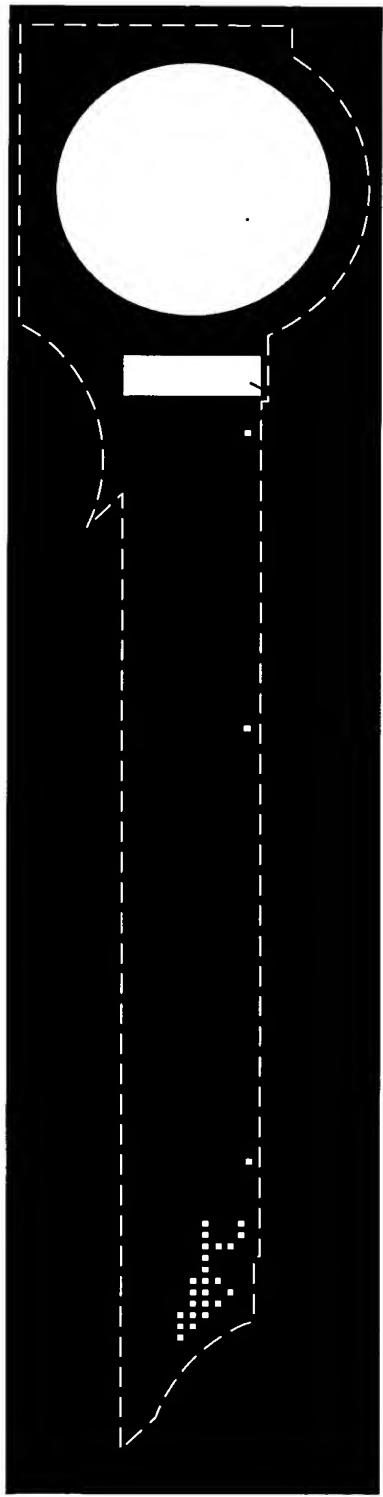
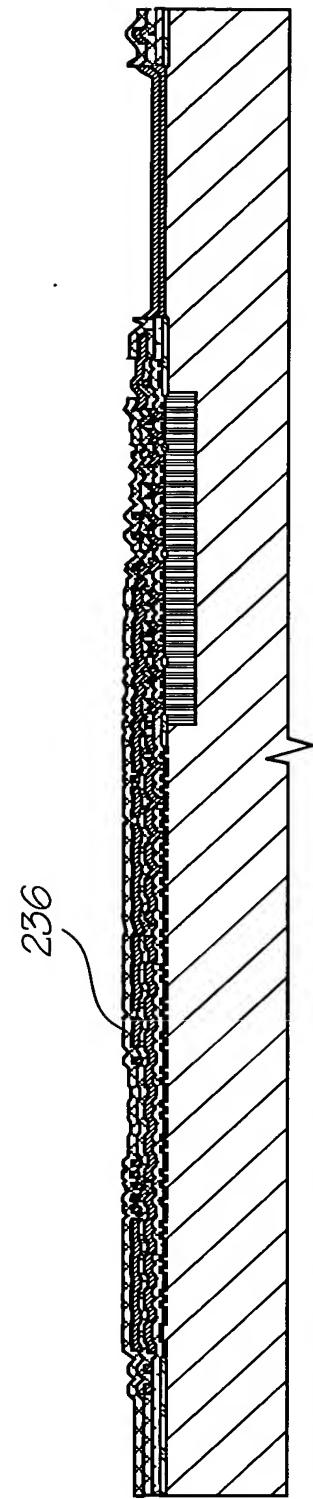


FIG. 44



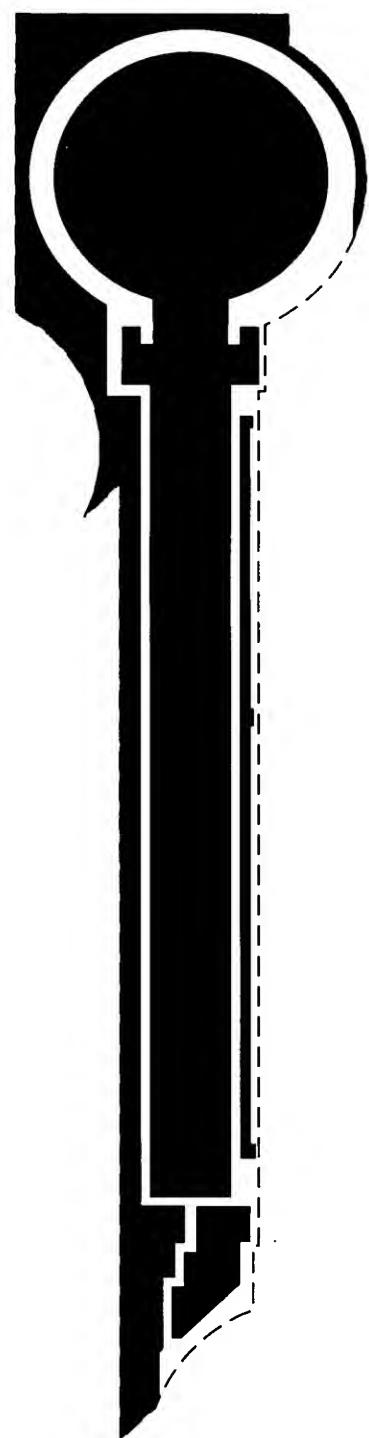
Via 2 mask

FIG. 45



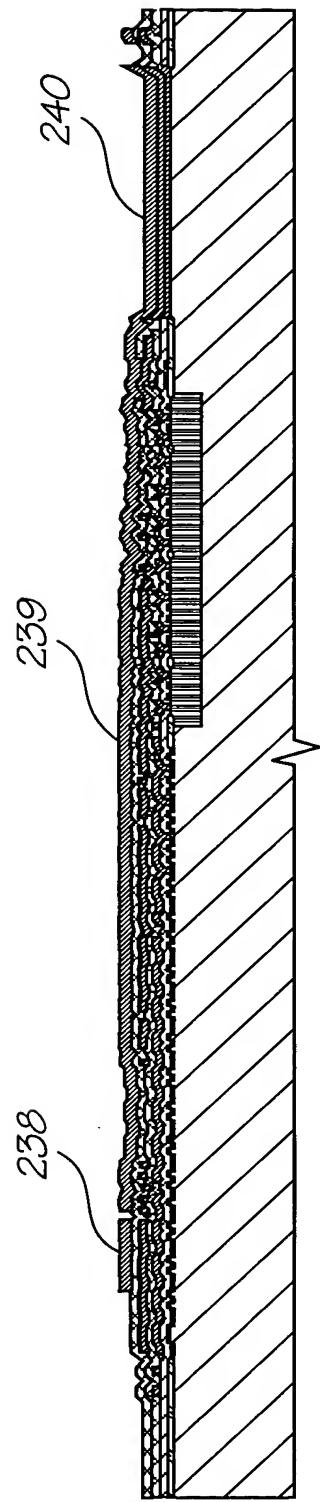
Deposit ILD 3, etch vias

FIG. 46



Metal 3 mask

FIG. 47



Deposit metal 3

FIG. 48

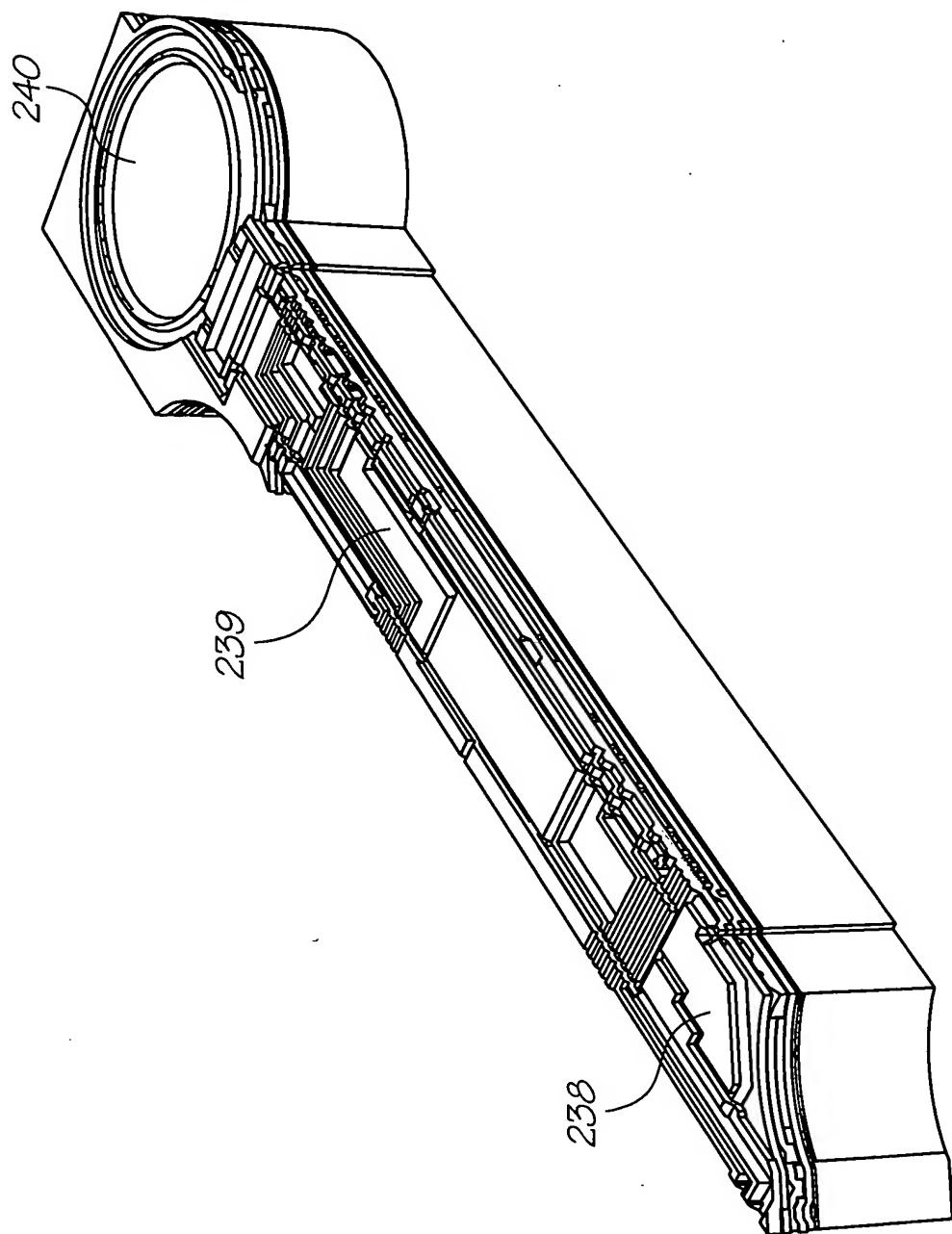
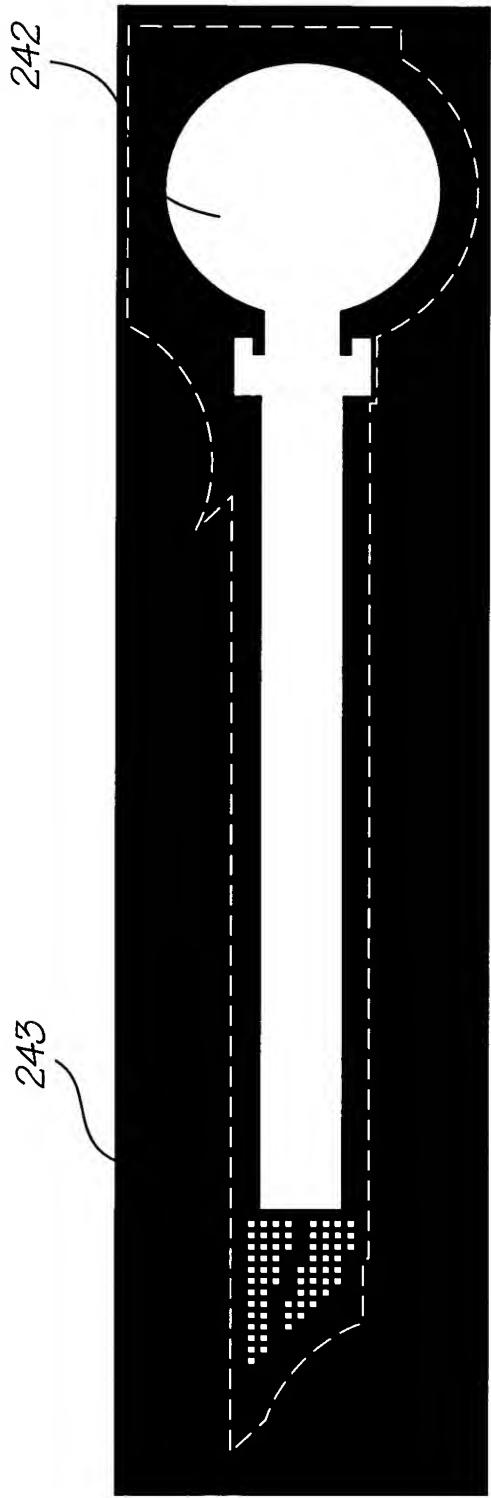
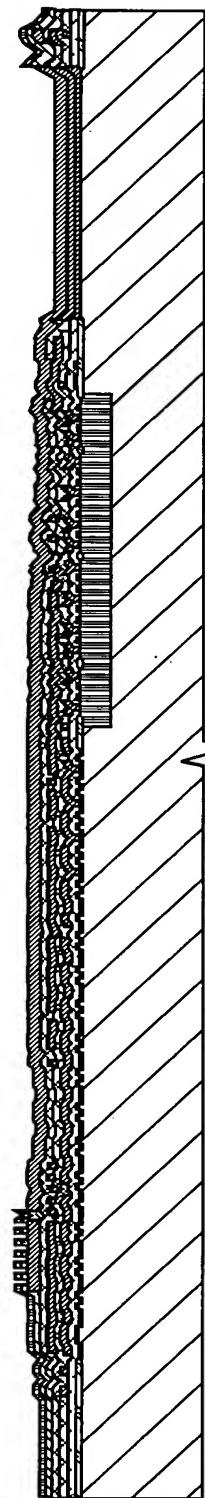


FIG. 4.9



Via 3 / Passivation mask

FIG. 50



Deposit passivation oxide & nitride, etch vias

FIG. 51

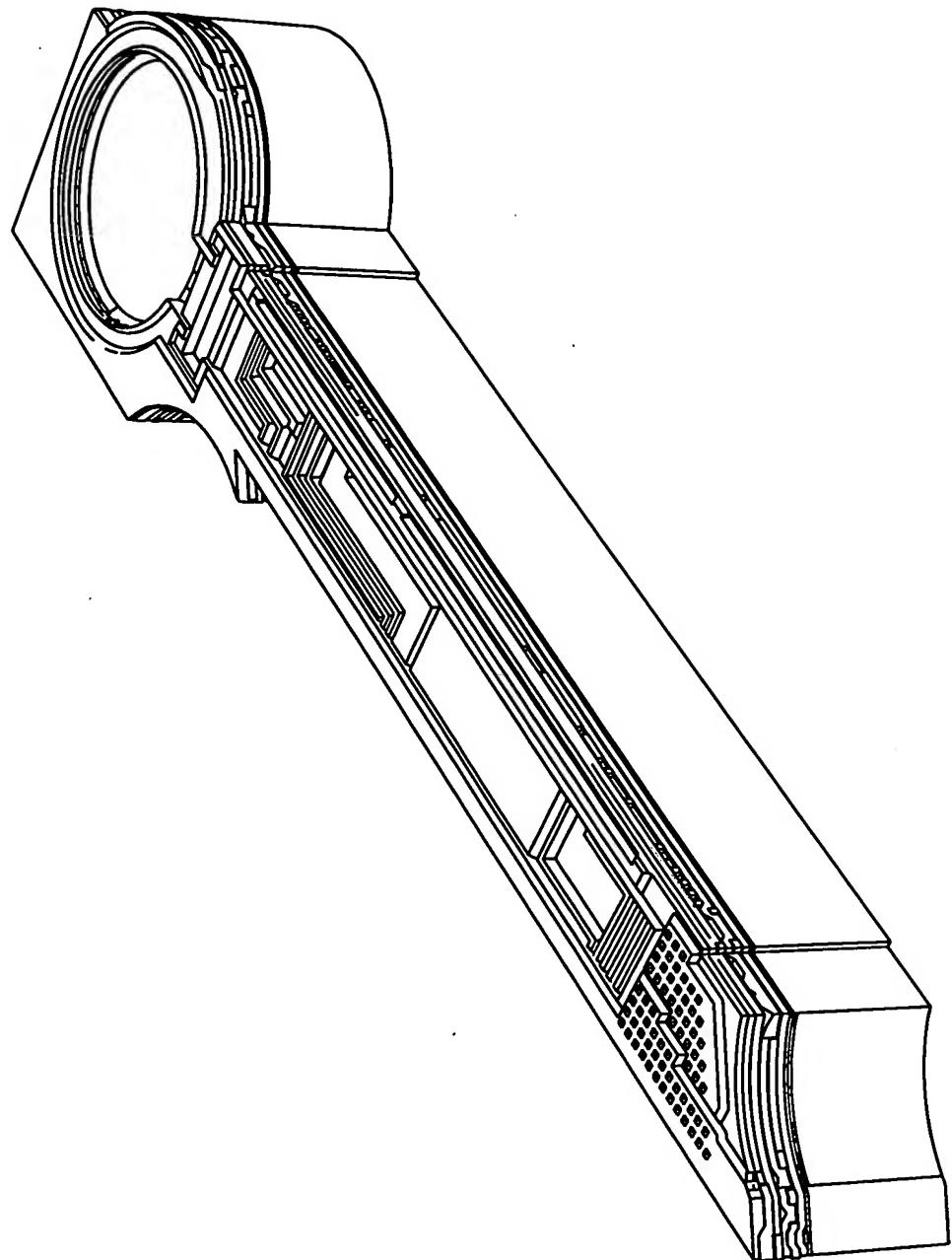
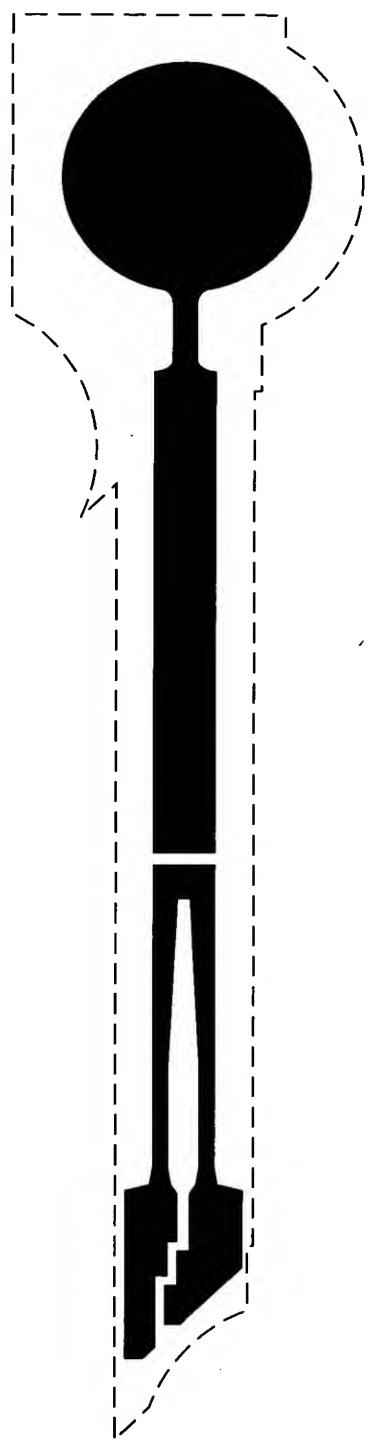
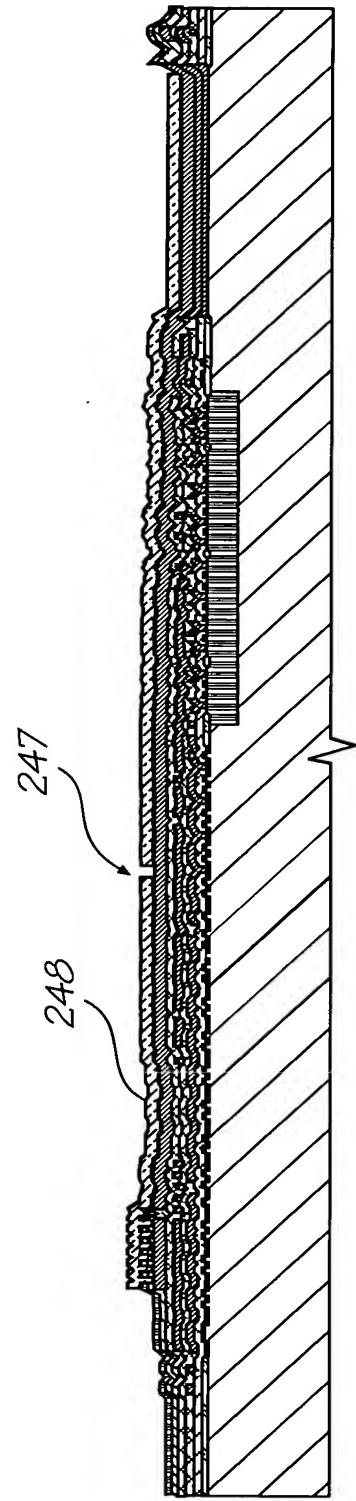


FIG. 52



Heater mask

FIG. 53



Deposit heater TiN

FIG. 54

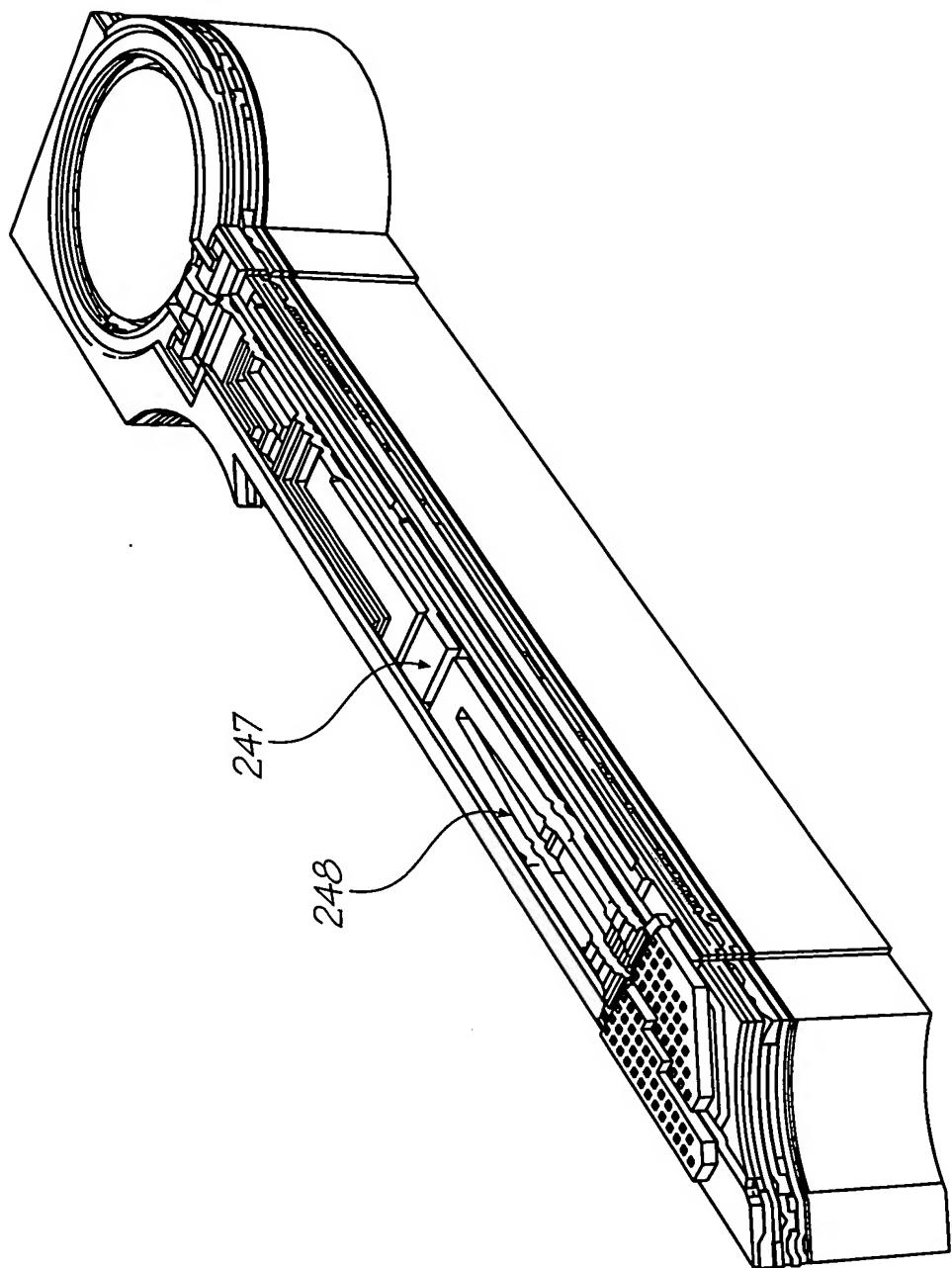


FIG. 55

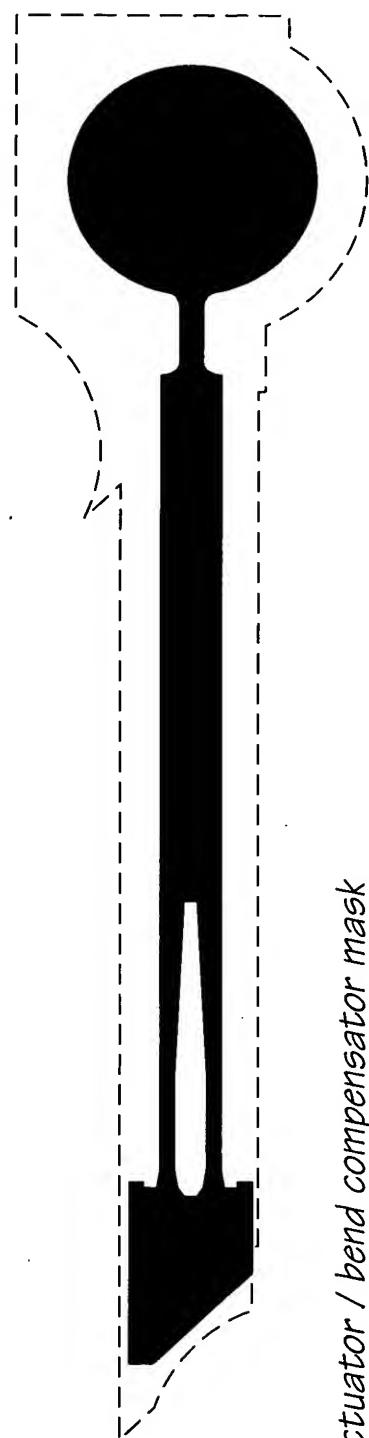


FIG. 56

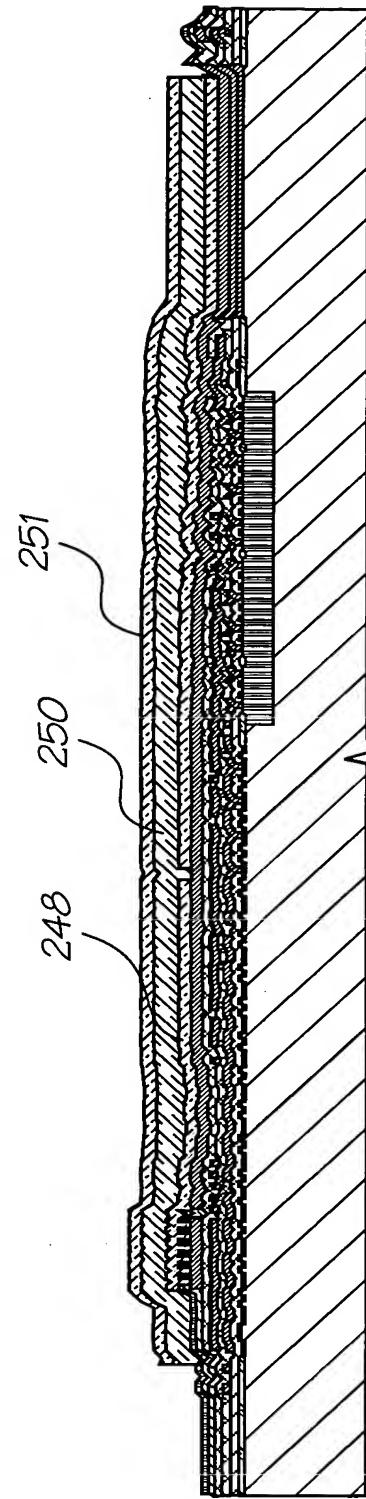


FIG. 57

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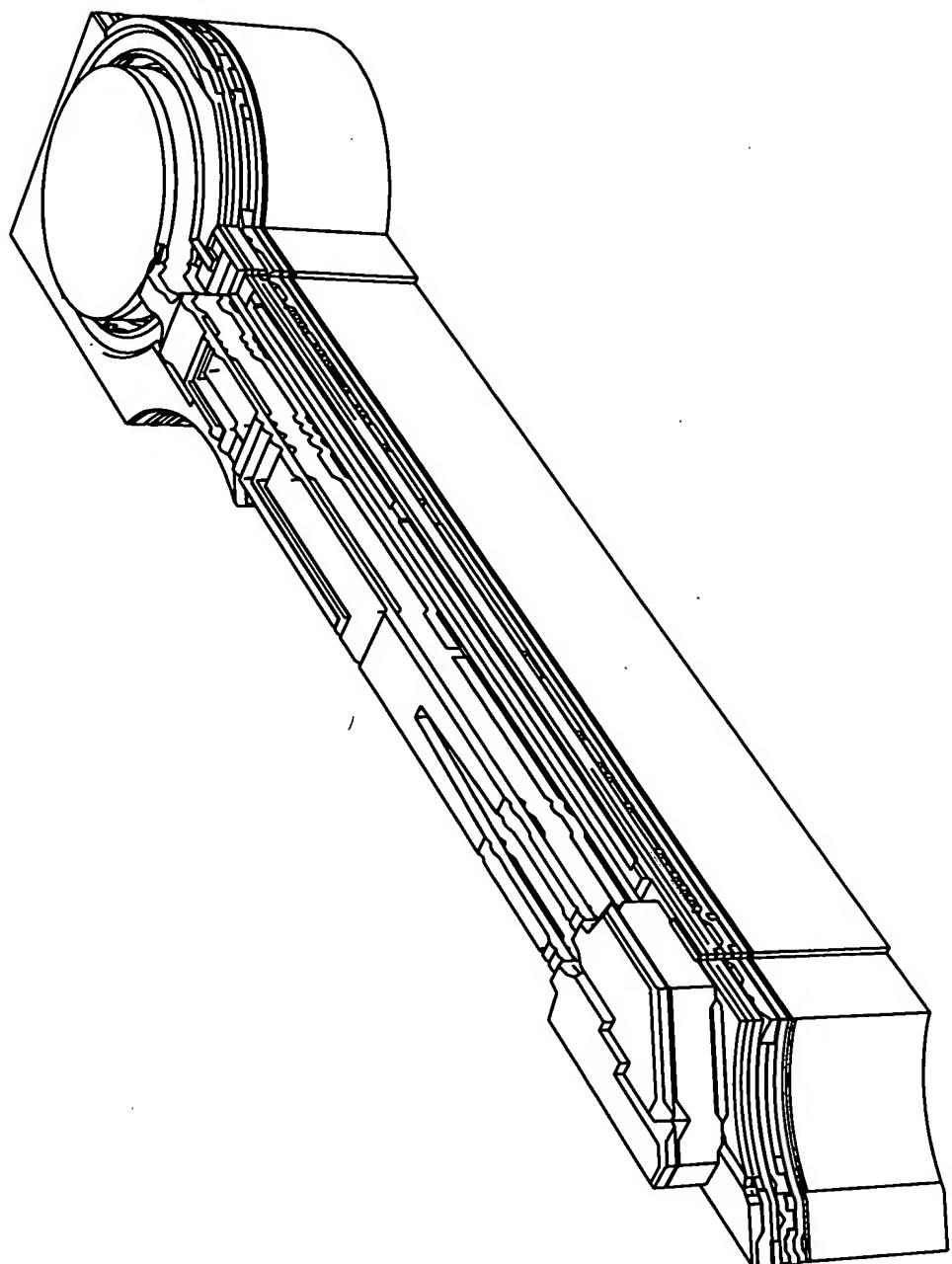
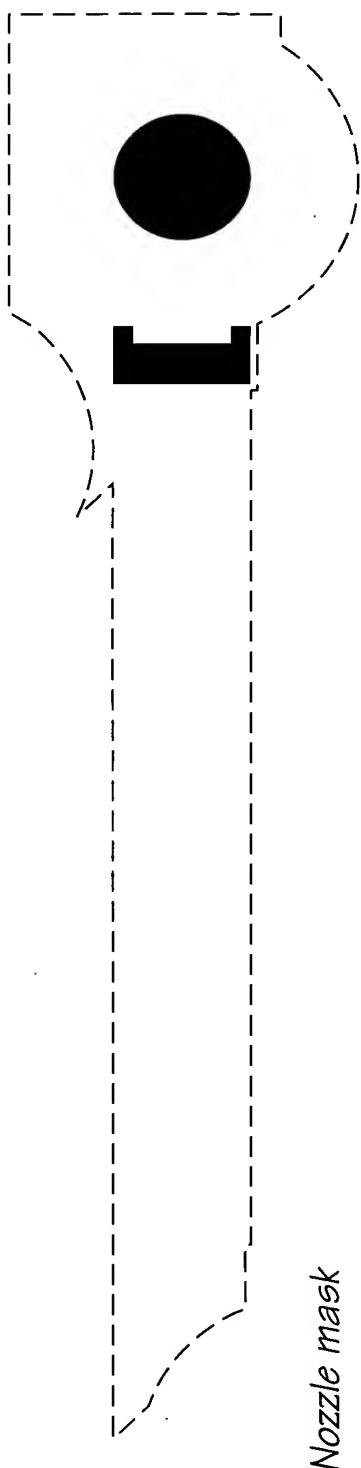
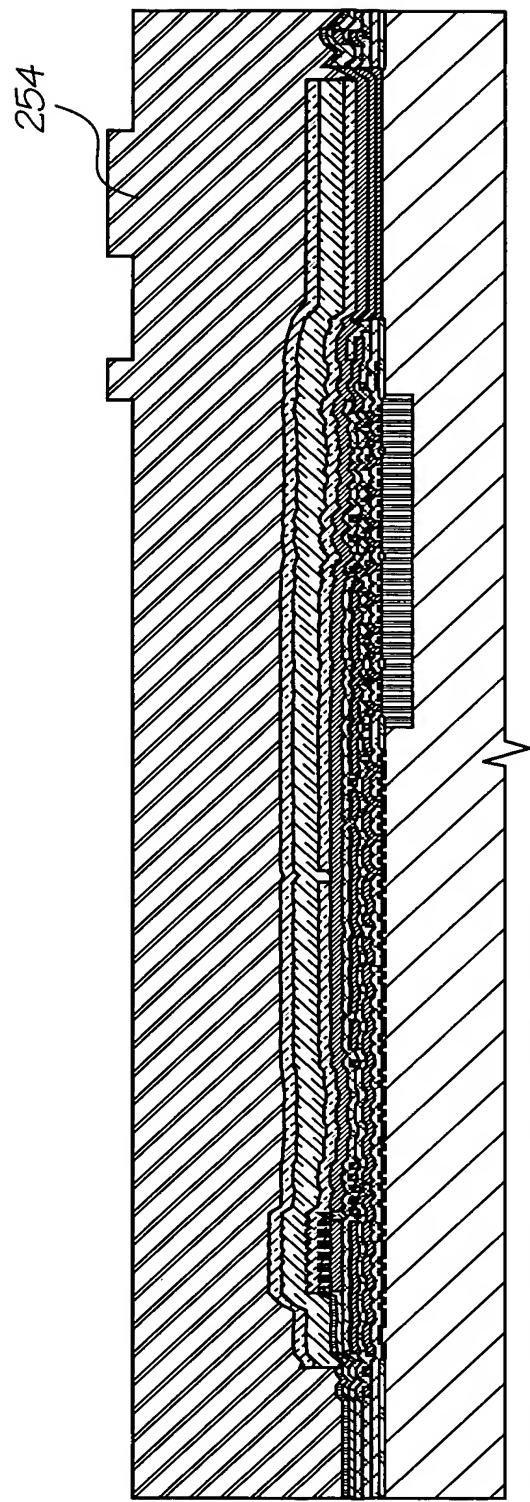


FIG. 58



Nozzle mask

FIG. 59



Deposit sacrificial layer, etch nozzles

FIG. 60

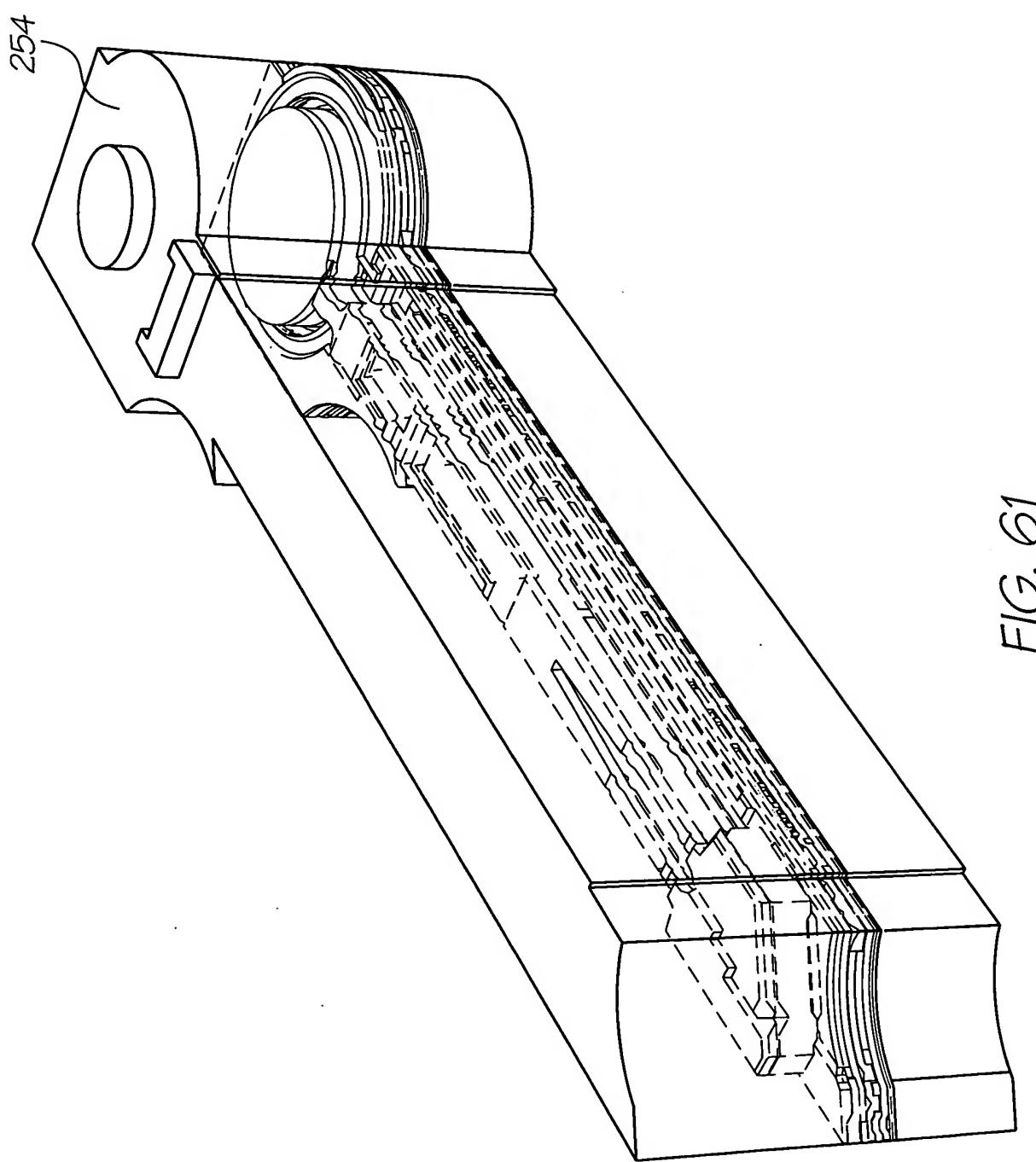
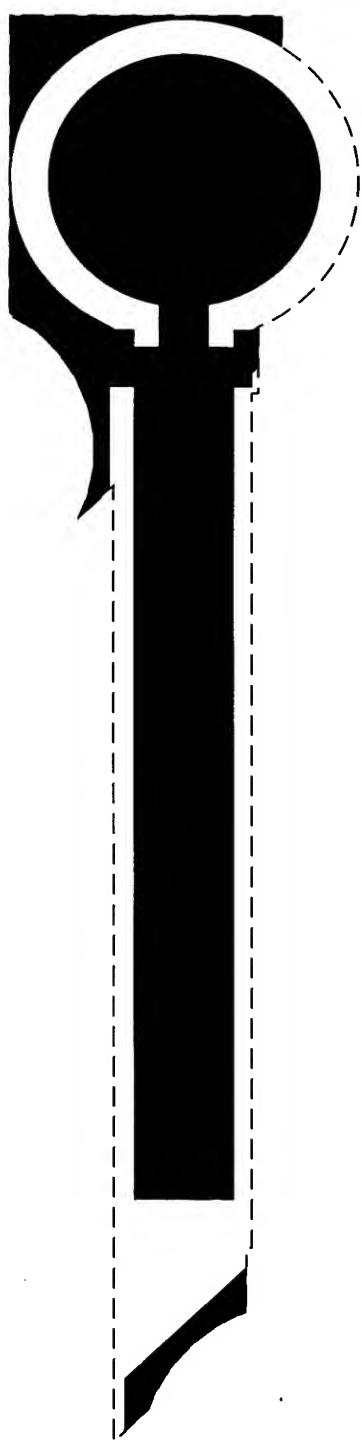
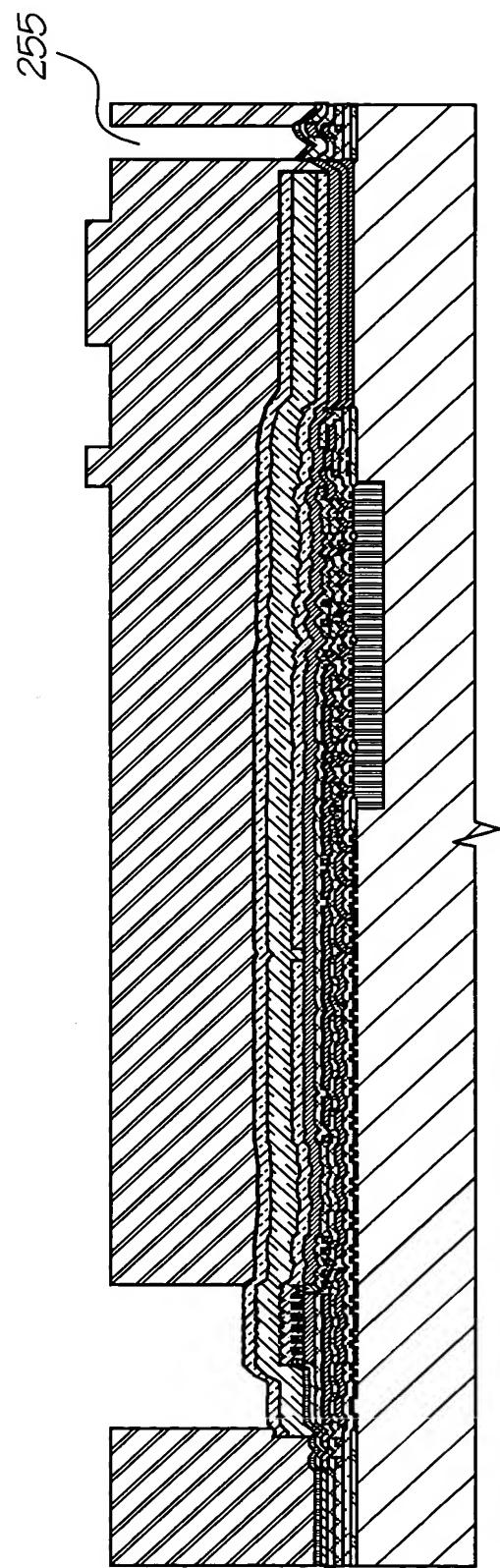


FIG. 61



Chamber mask

FIG. 62



Etch chambers in sacrificial layer

FIG. 63

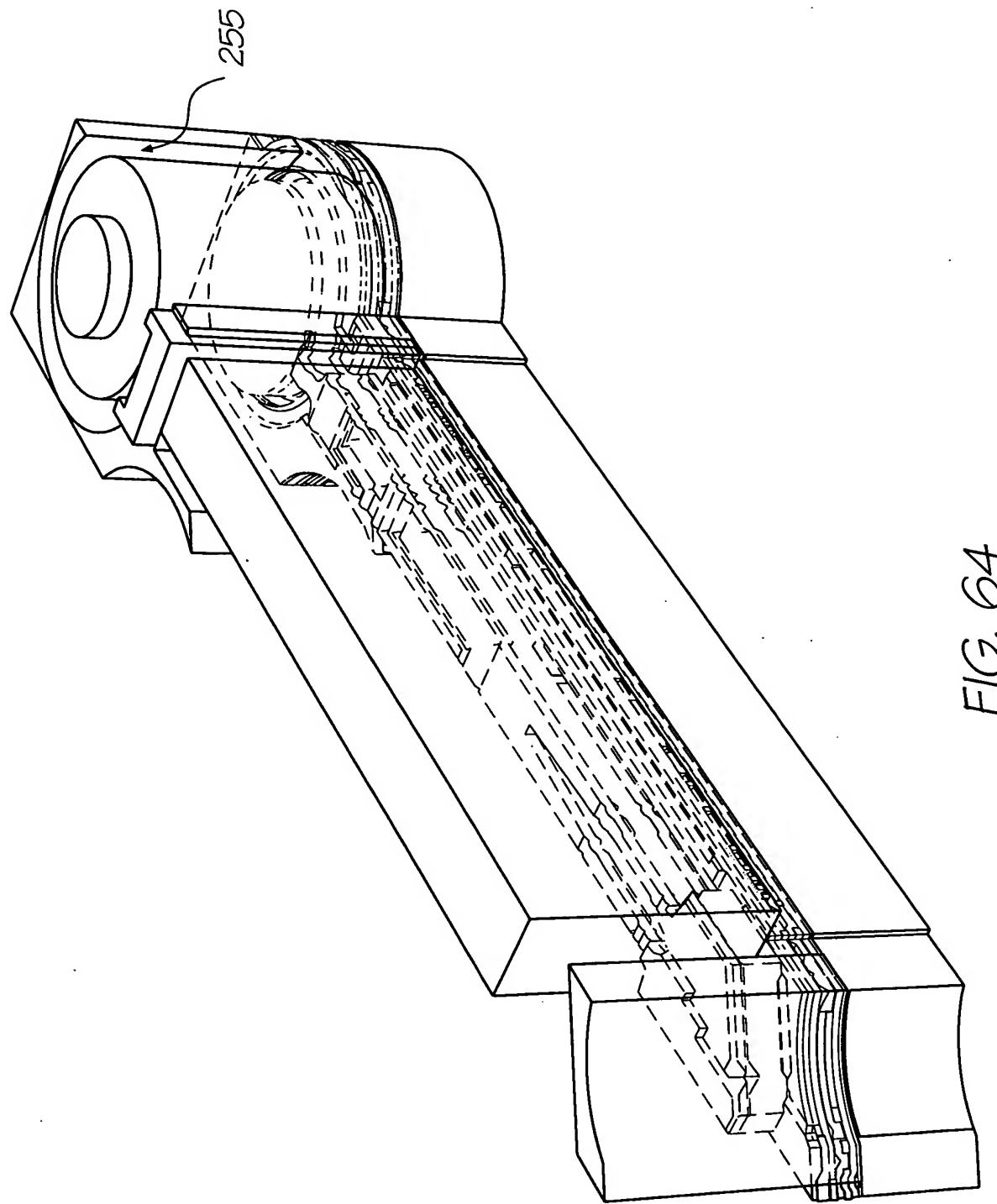


FIG. 64

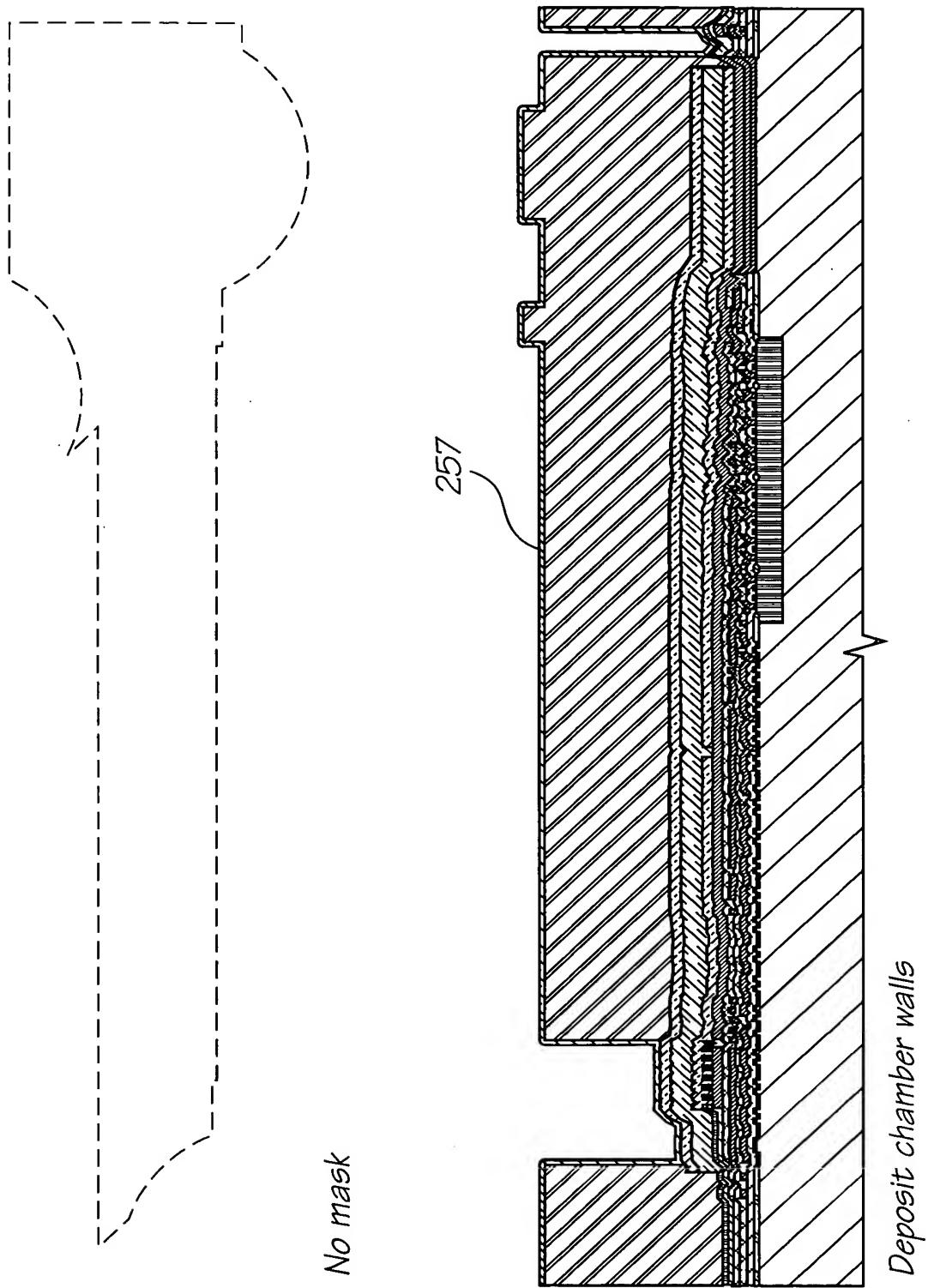
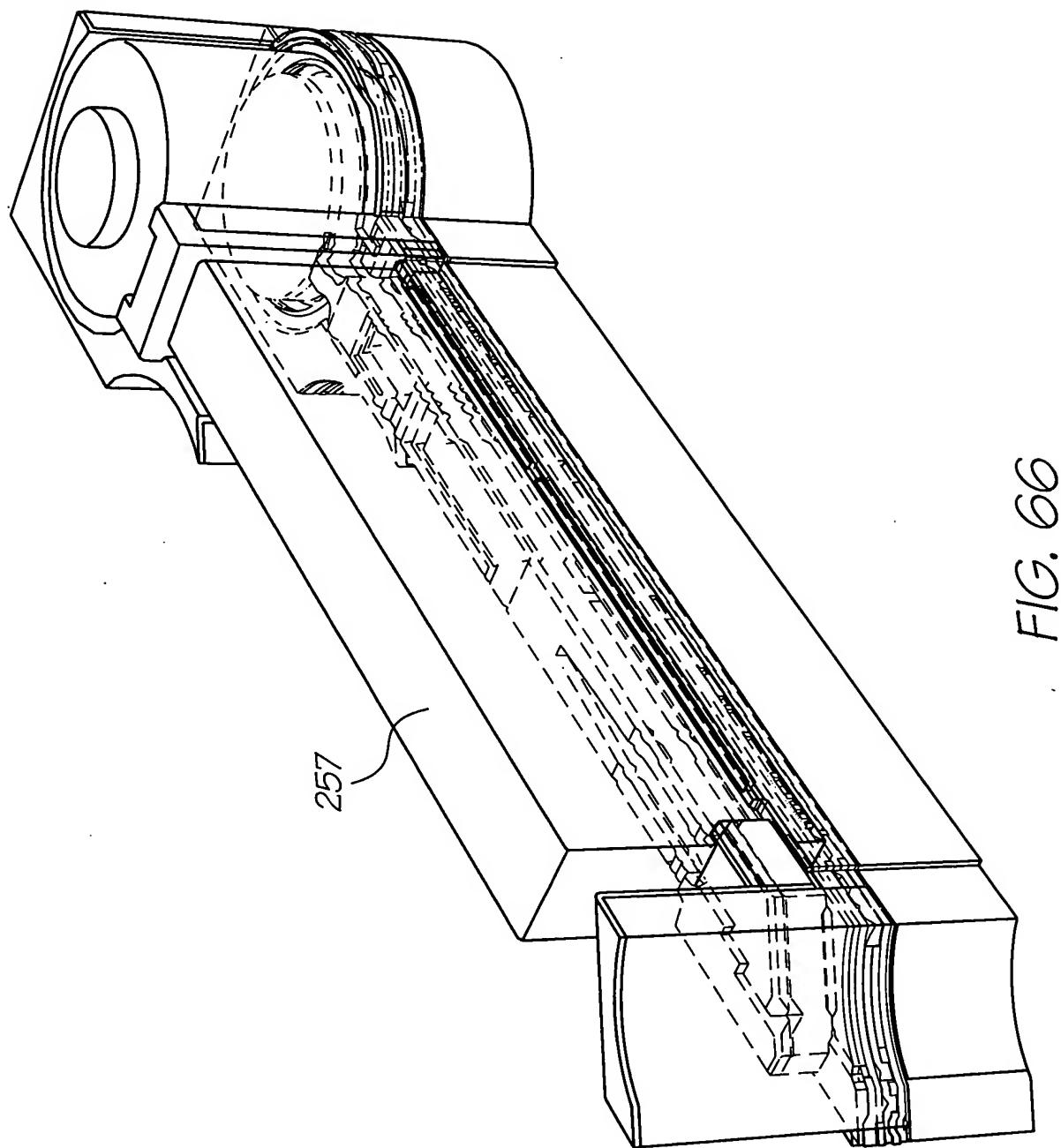


FIG. 65



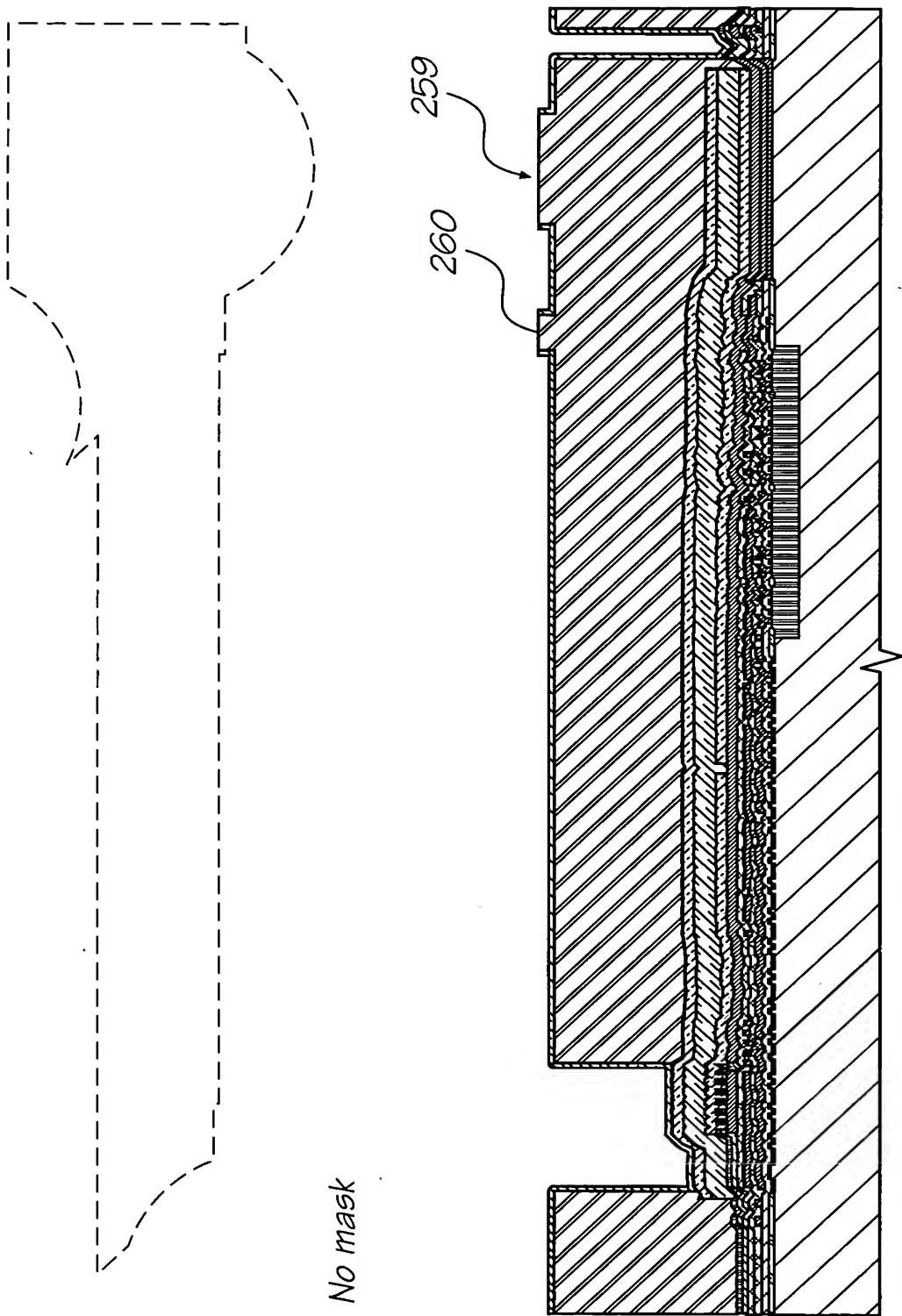


FIG. 67

Form self-aligned nozzles using CMP

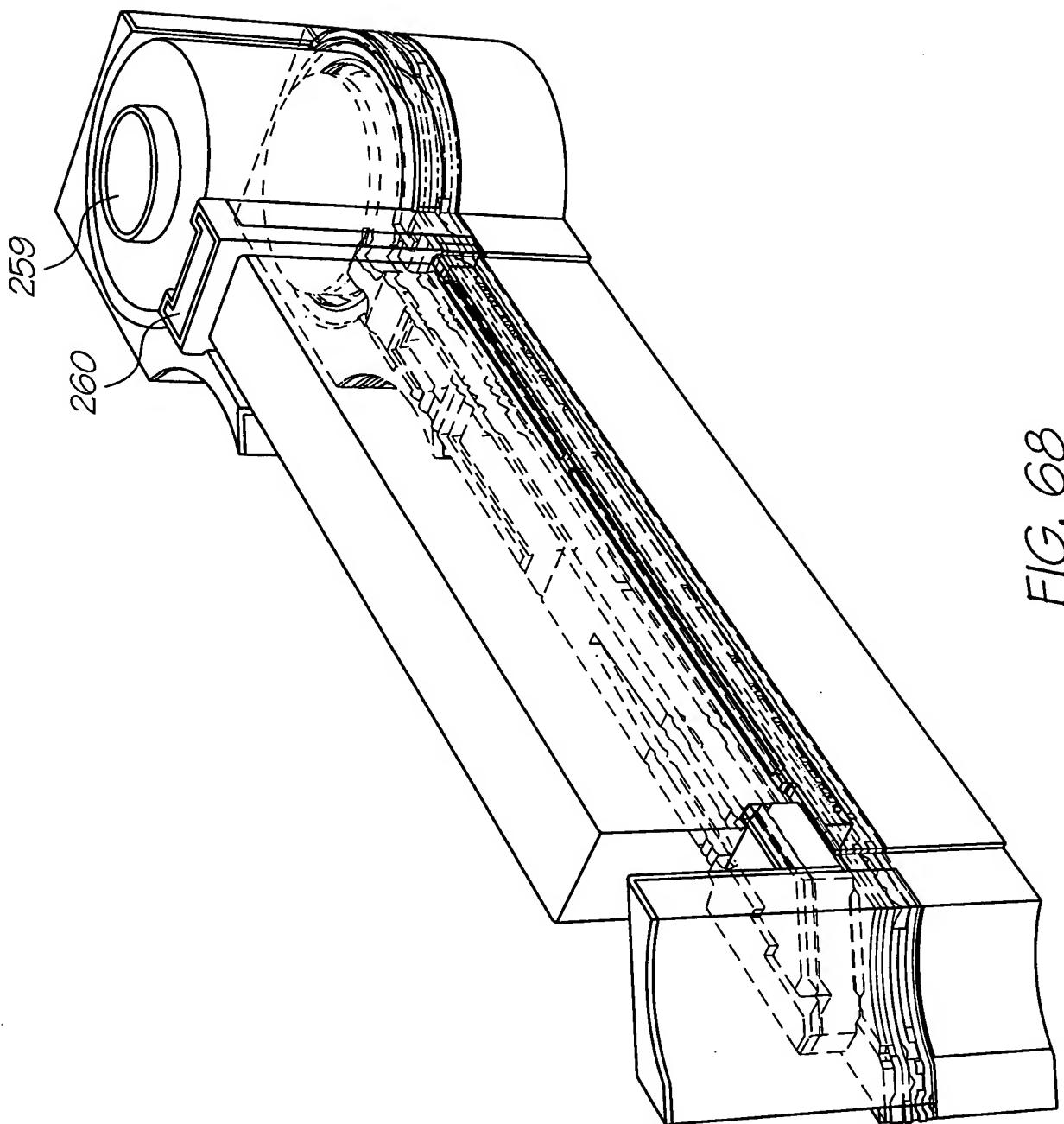


FIG. 68

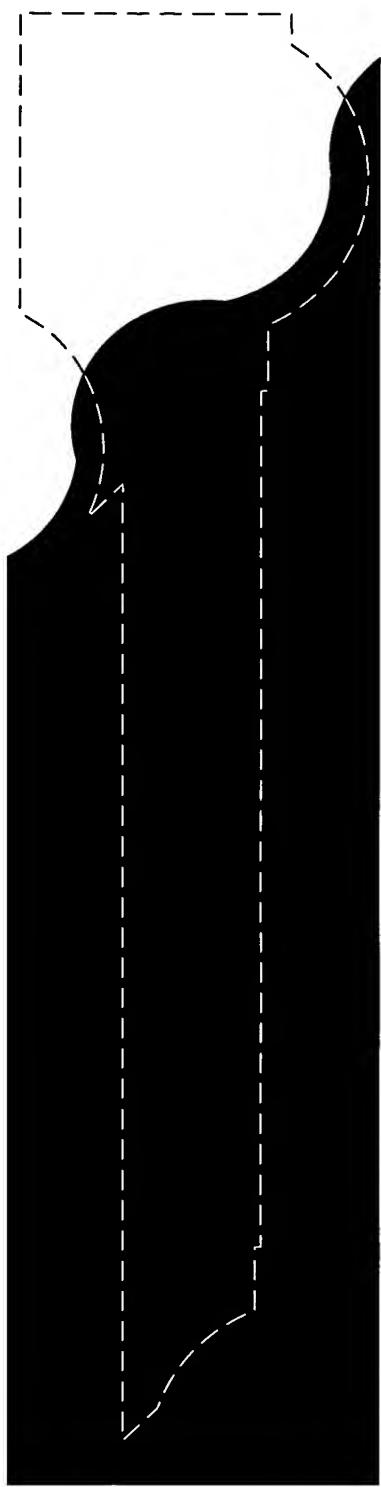


FIG. 70  
Back-etch inlet mask

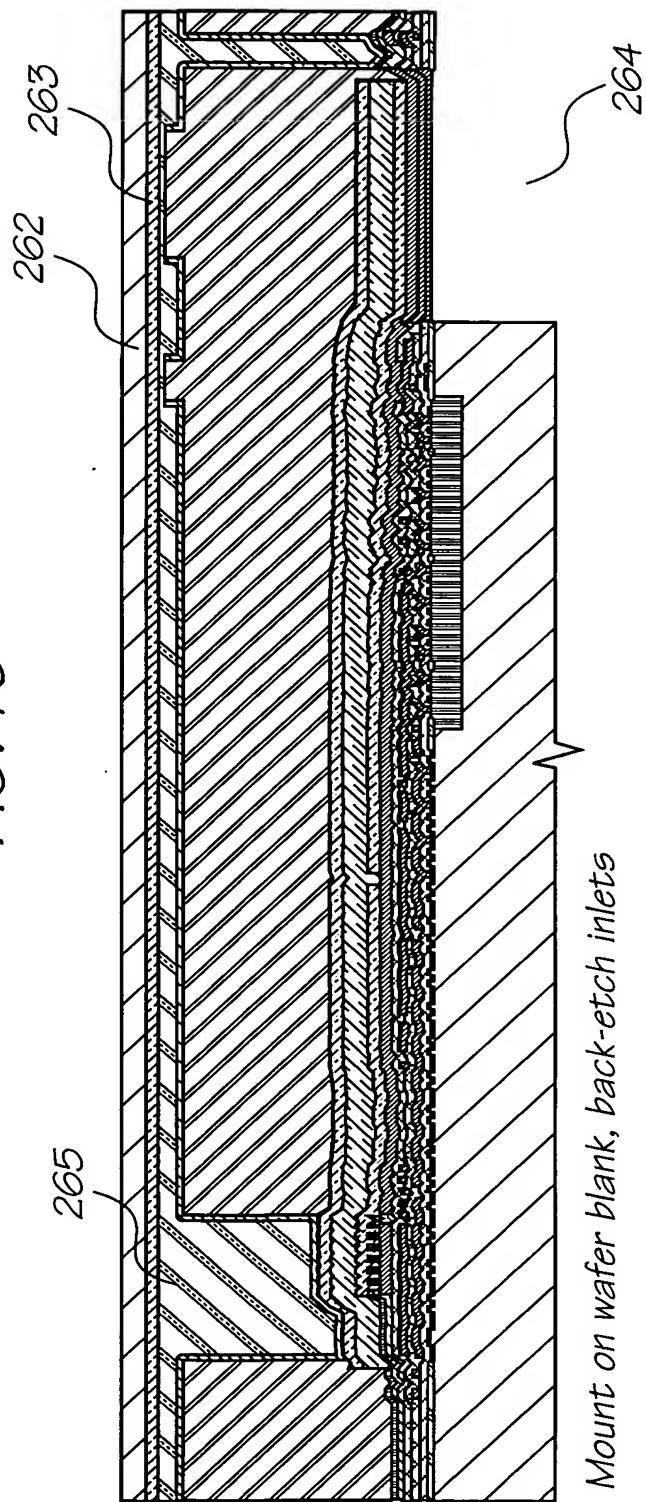


FIG. 69

Mount on wafer blank, back-etch inlets

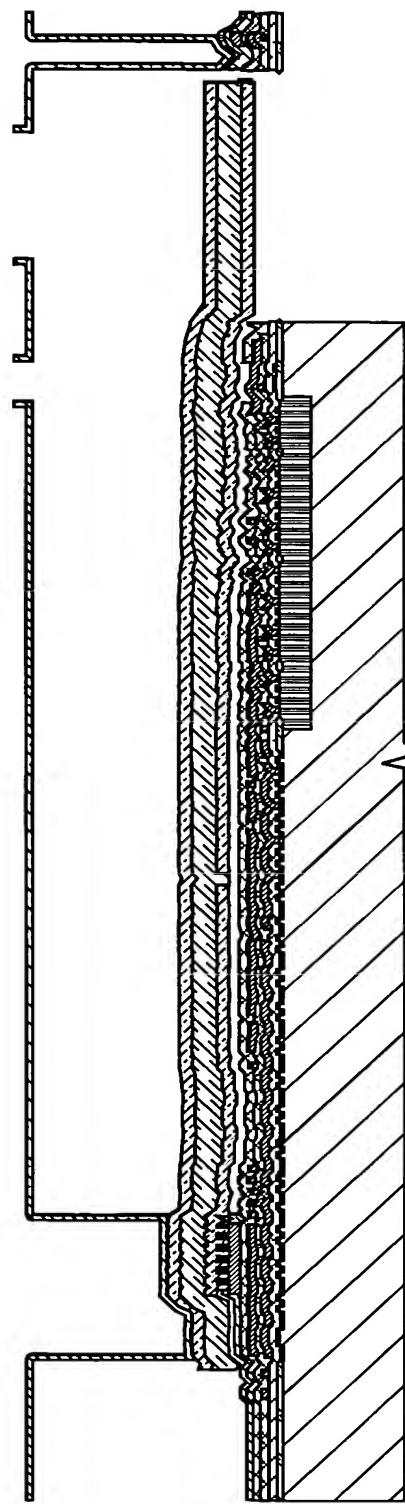
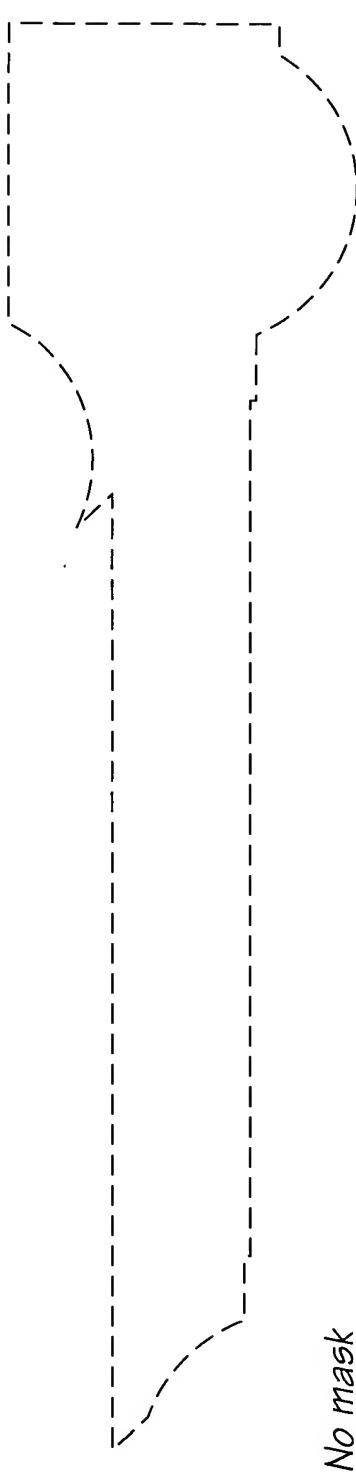


FIG. 71

*Detach from wafer blank, etch sacrificial material*

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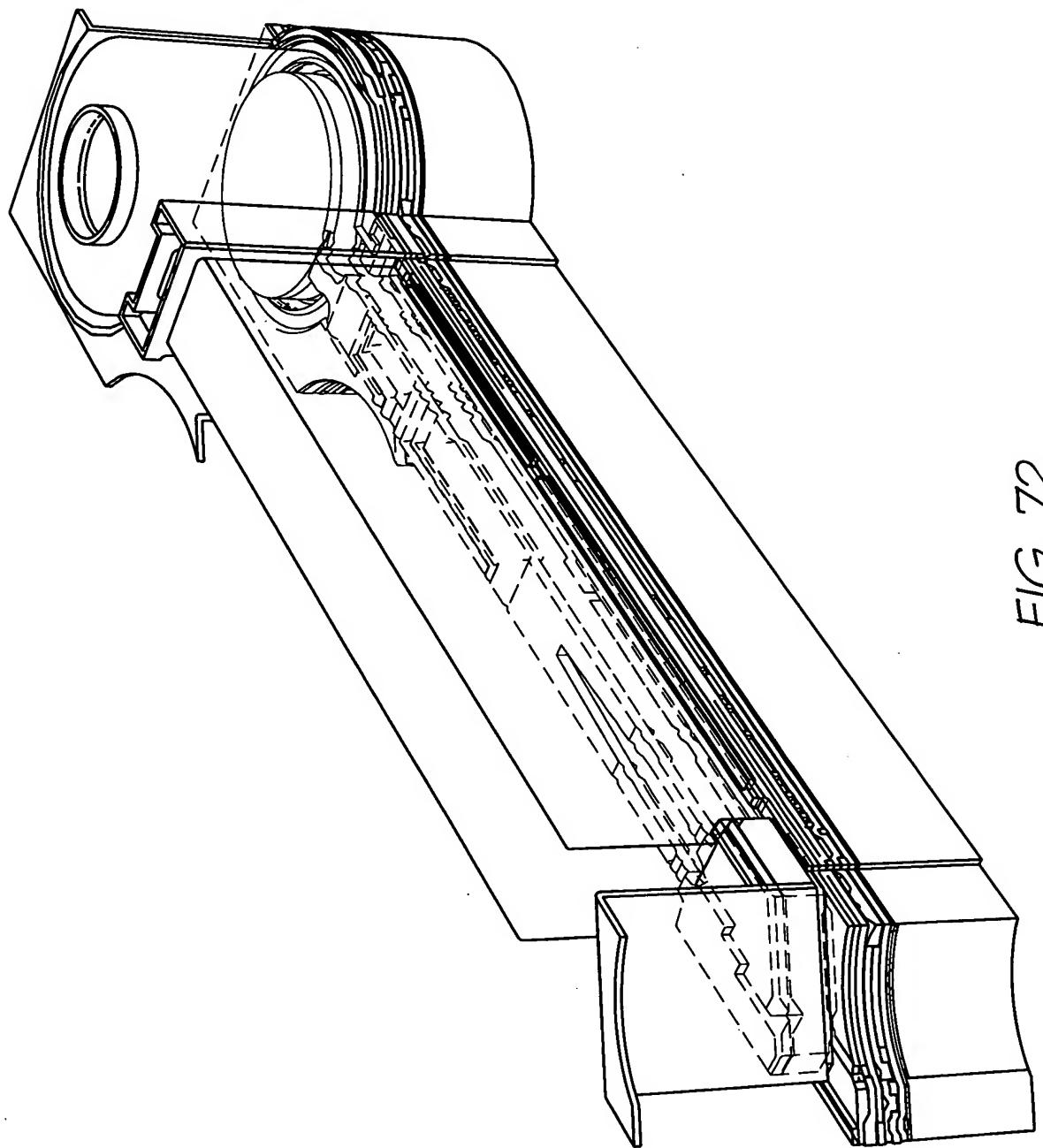


FIG. 72

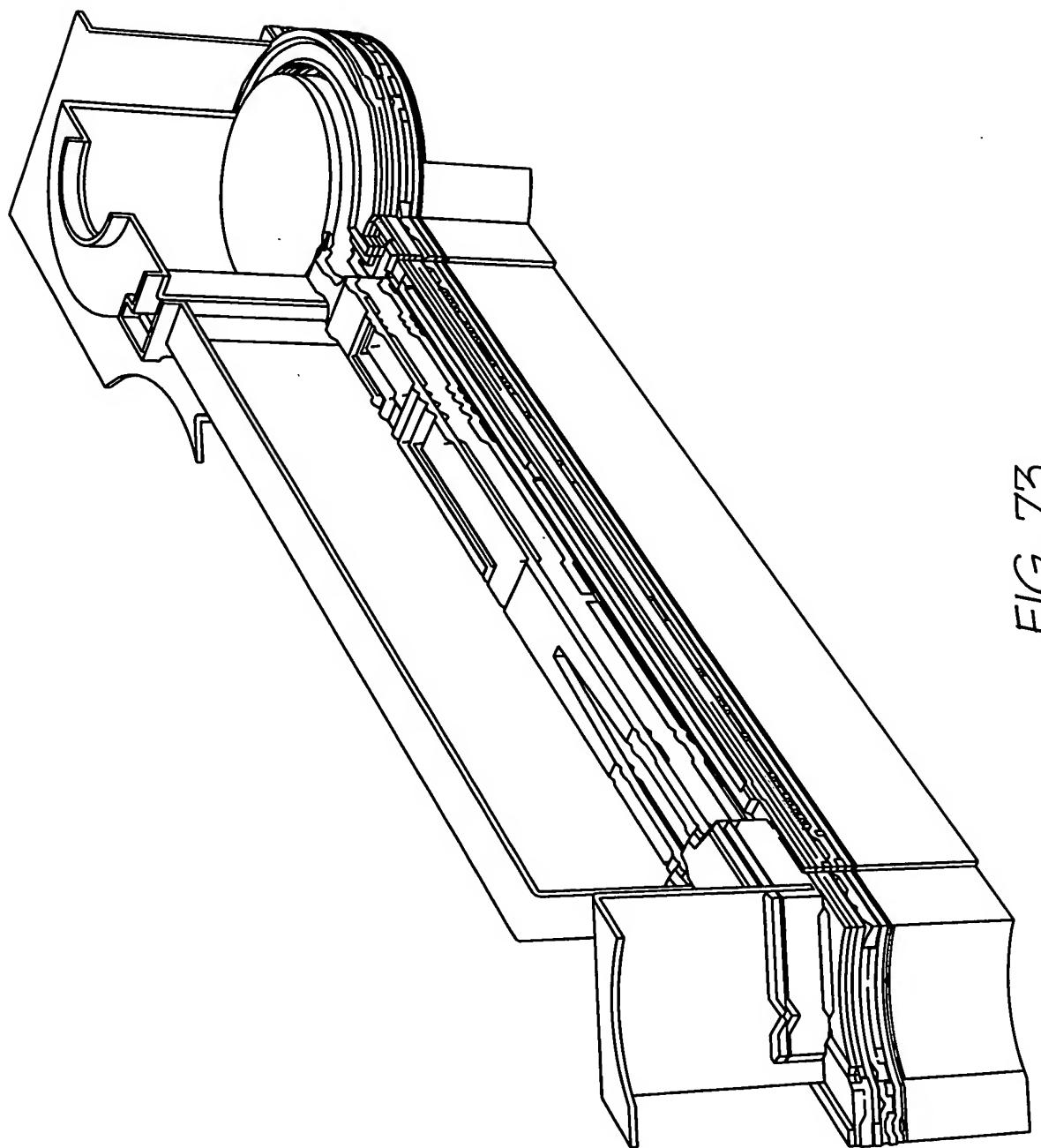


FIG. 73

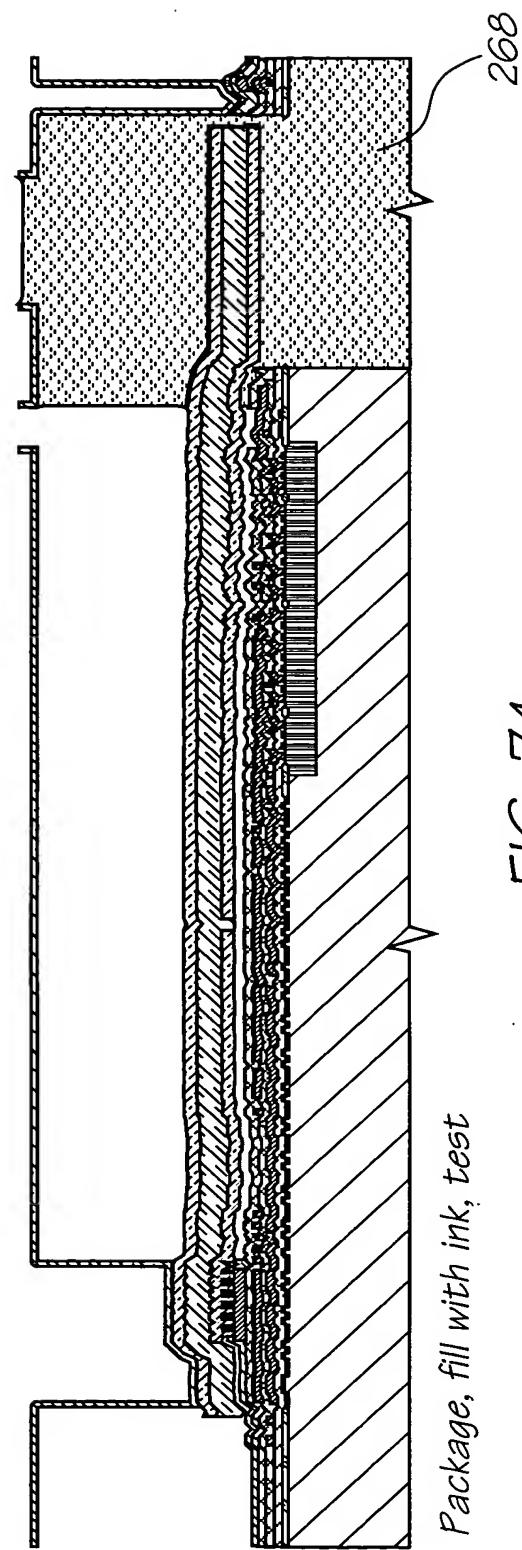
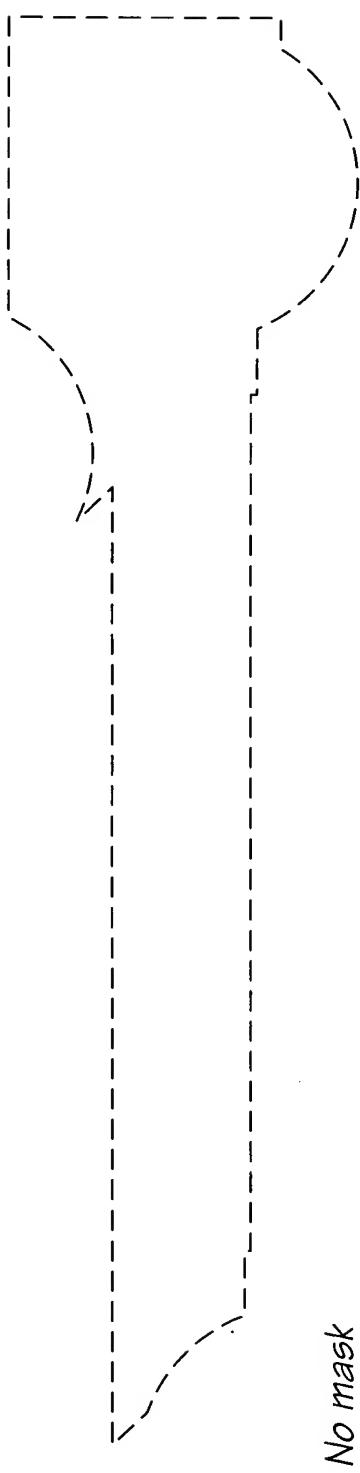


FIG. 74

Package, fill with ink, test

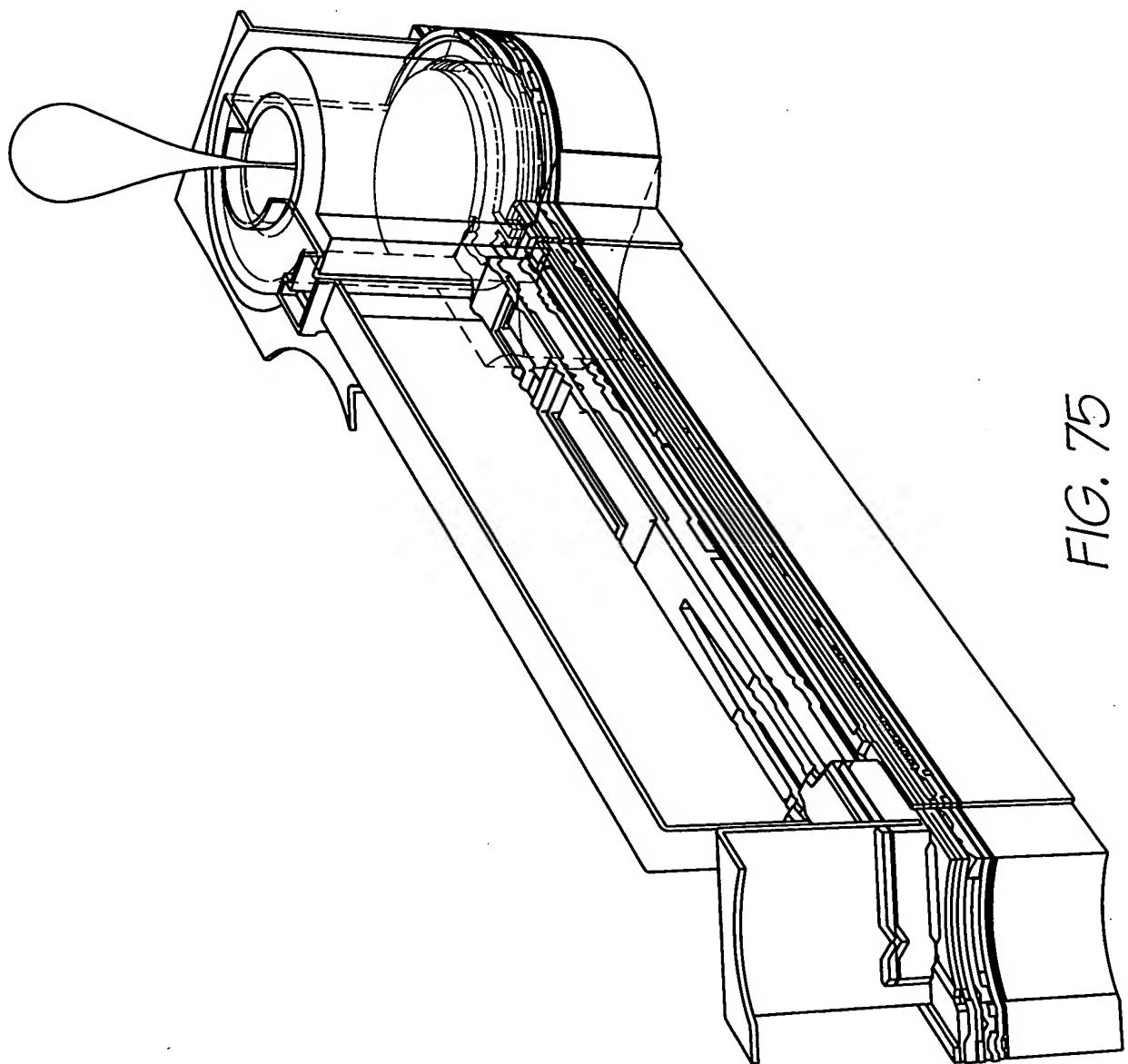


FIG. 75

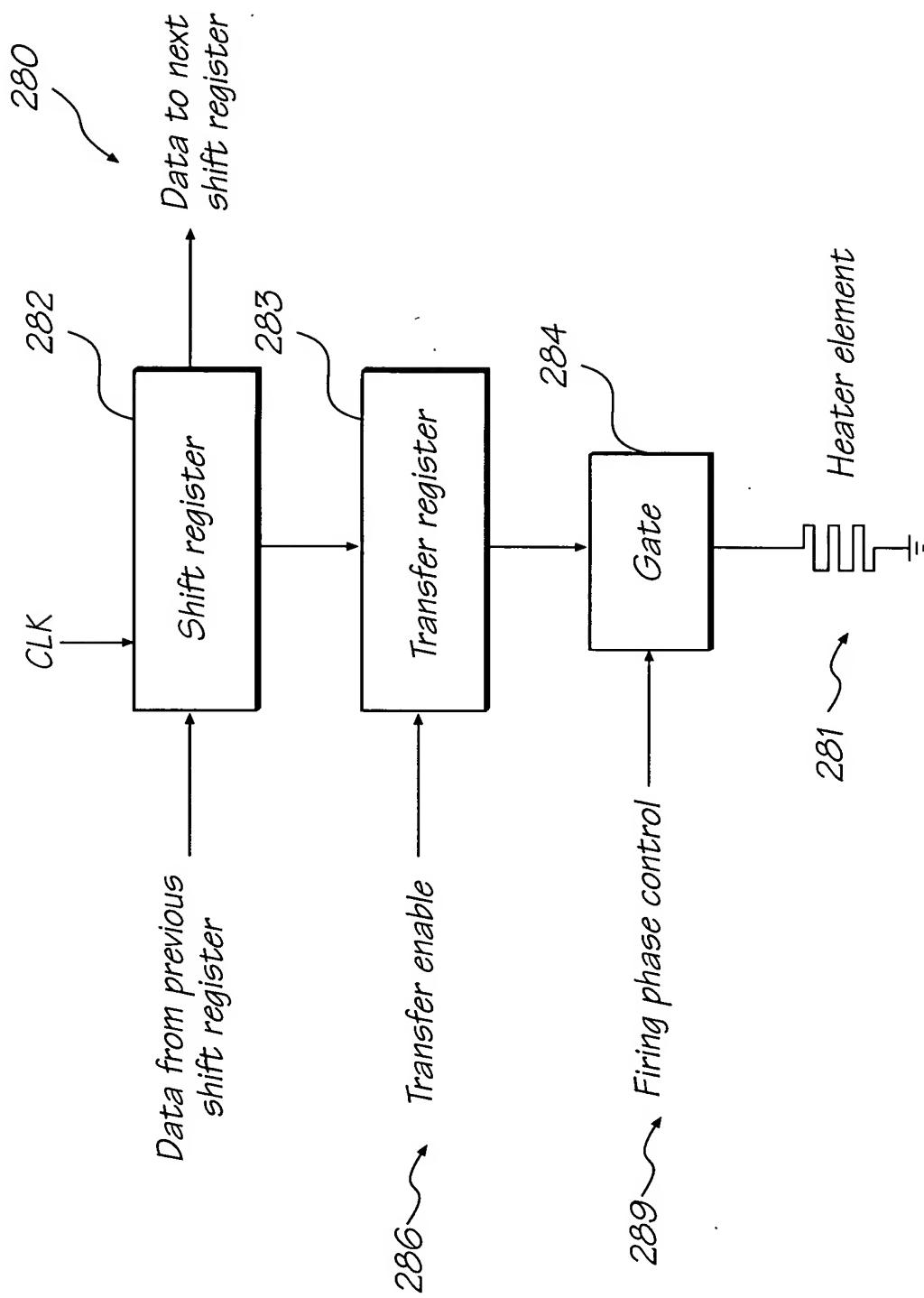


FIG. 76

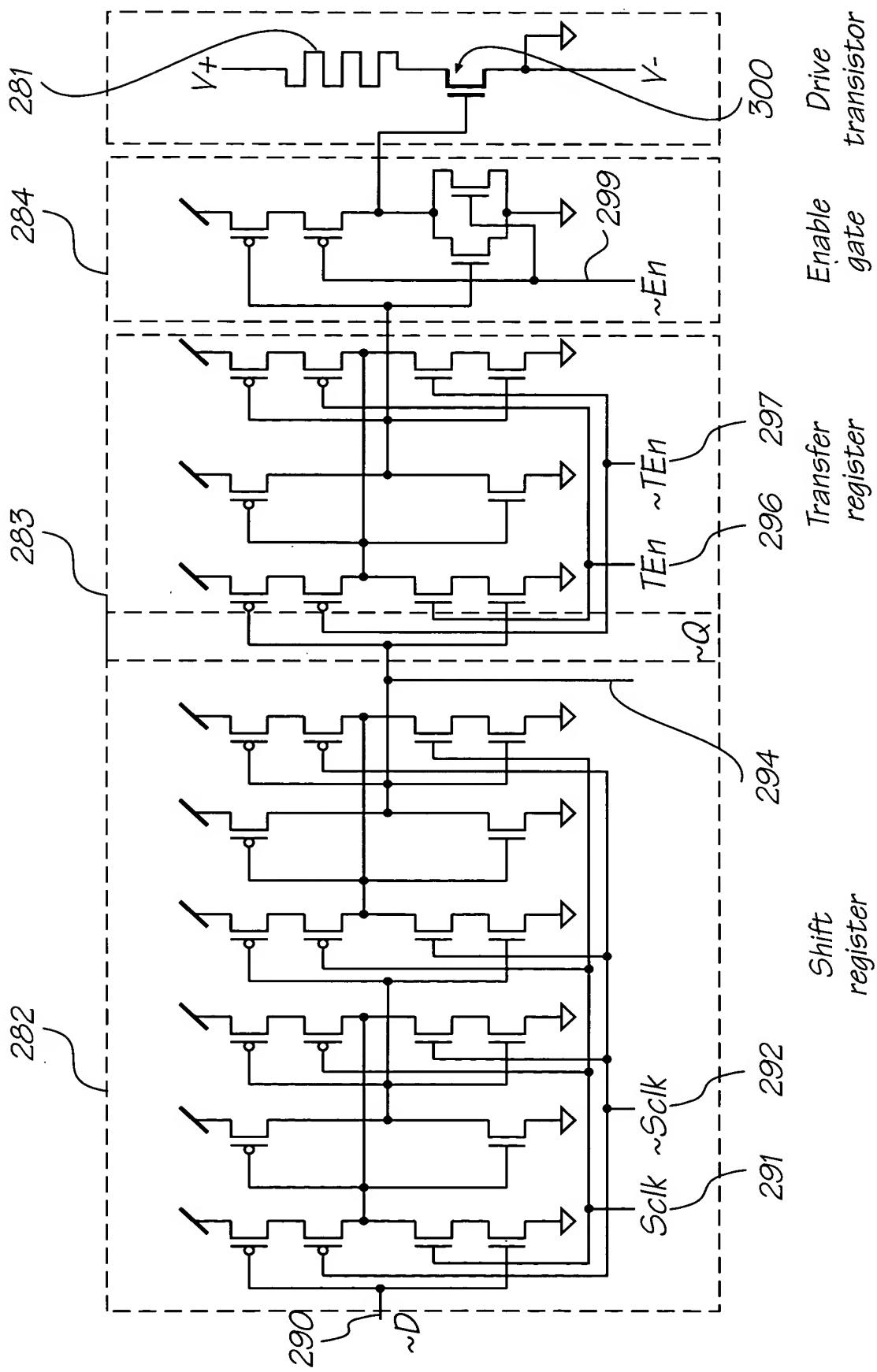


FIG. 77

Key

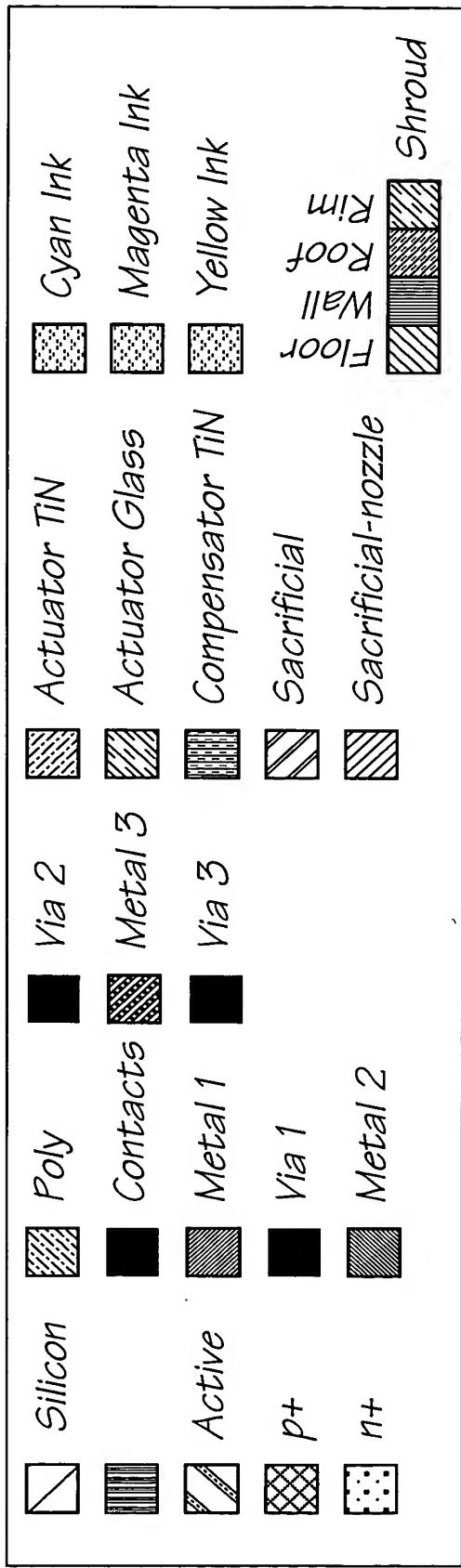


FIG. 78

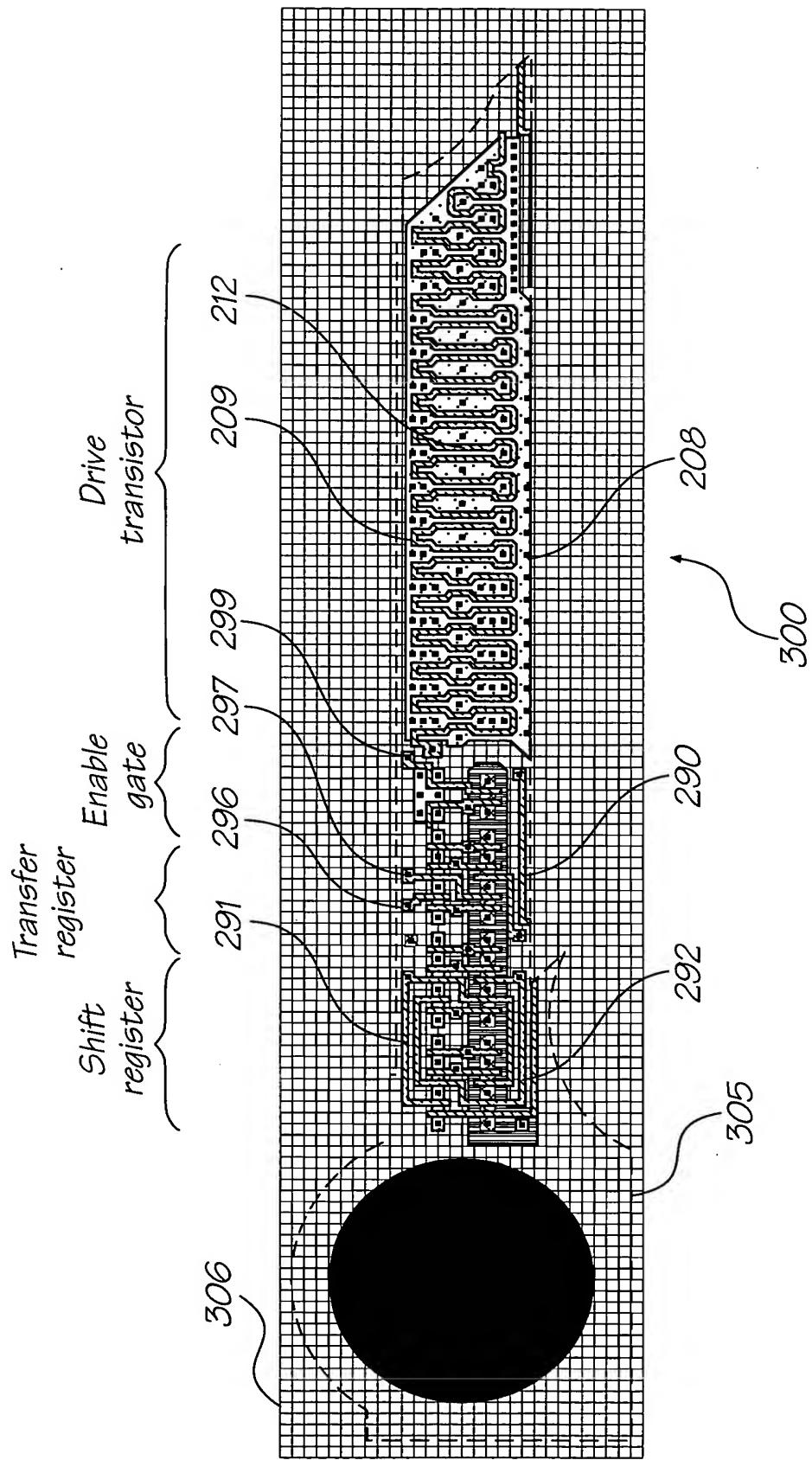


FIG. 79

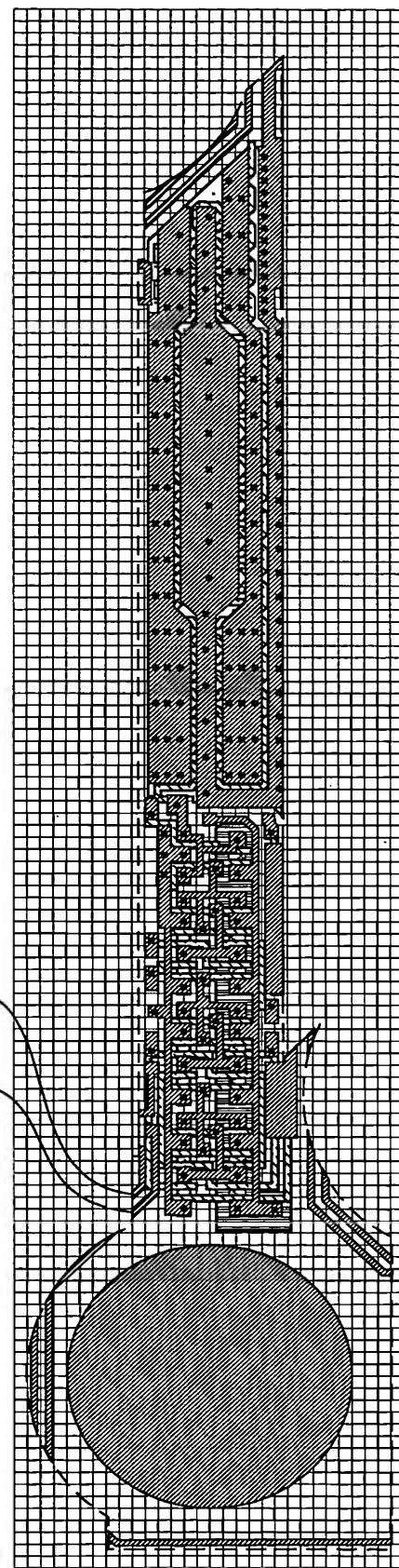


FIG. 80

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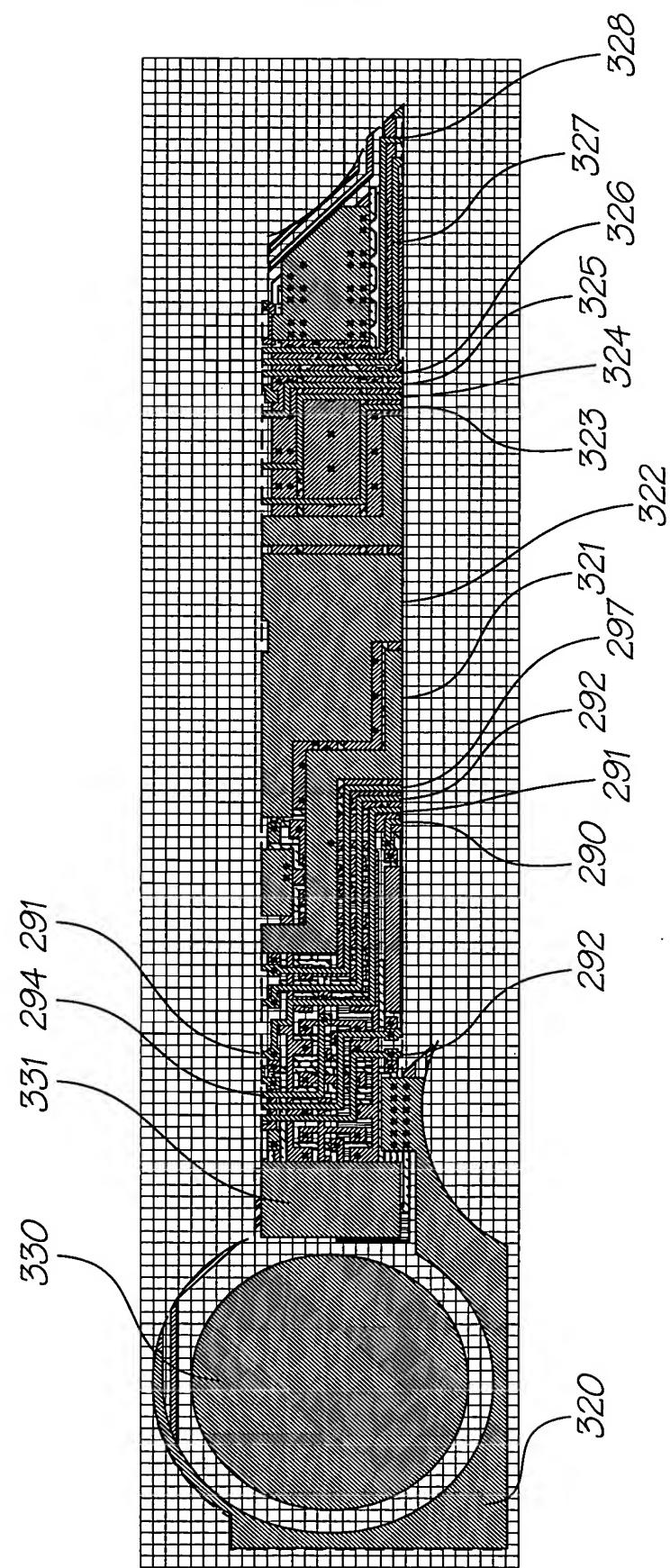


FIG. 81

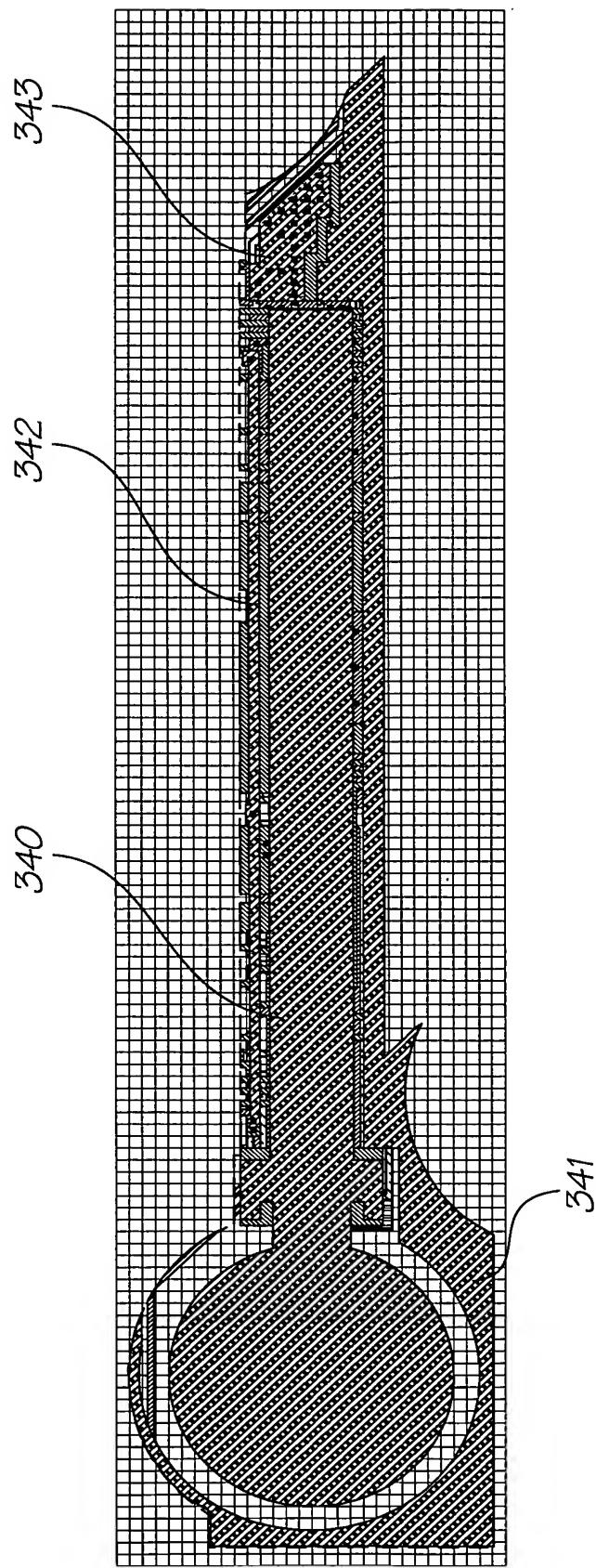


FIG. 82

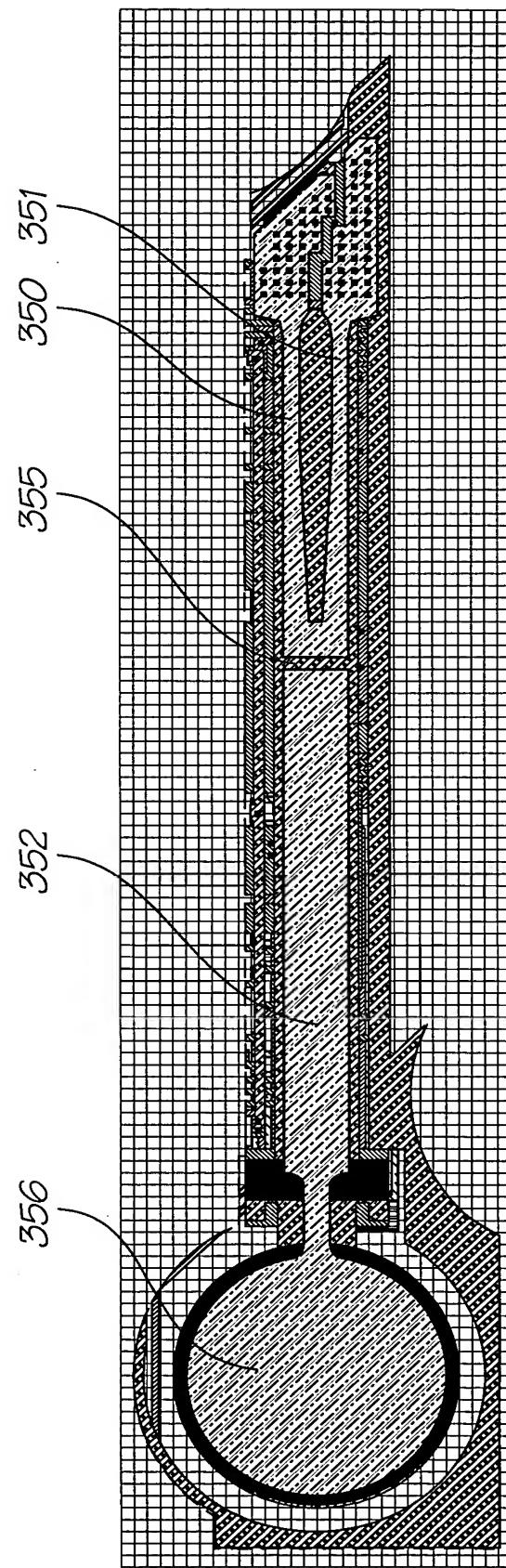


FIG. 83

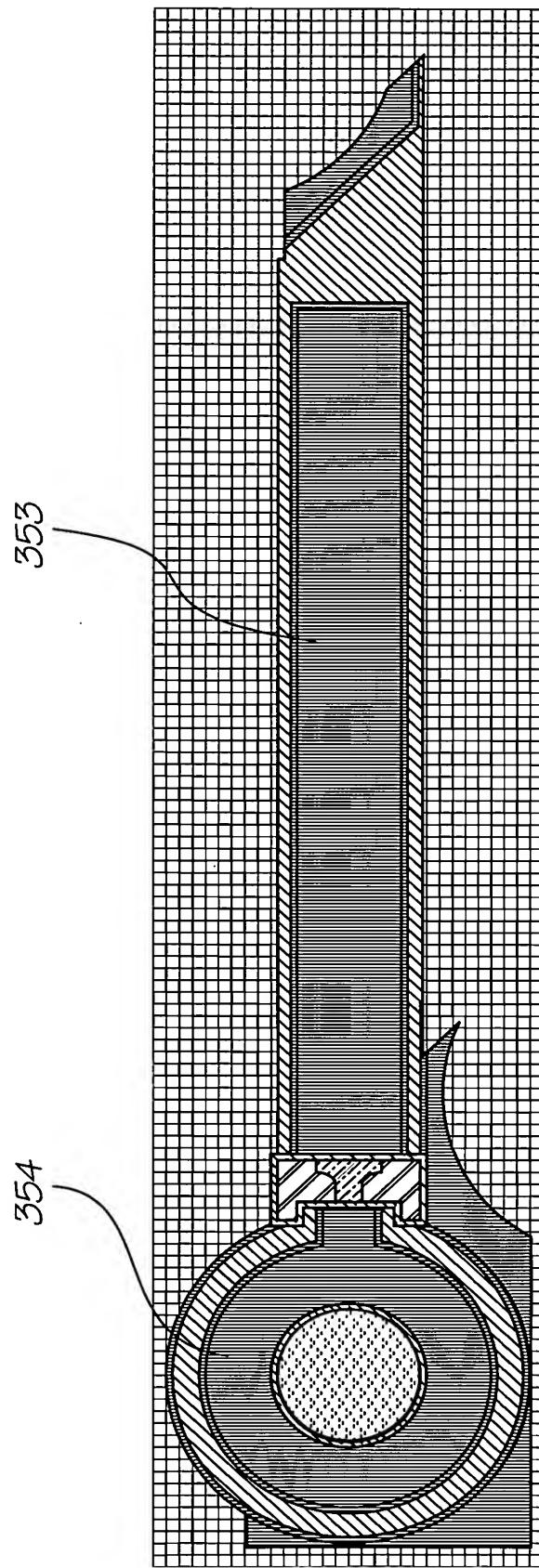


FIG. 84

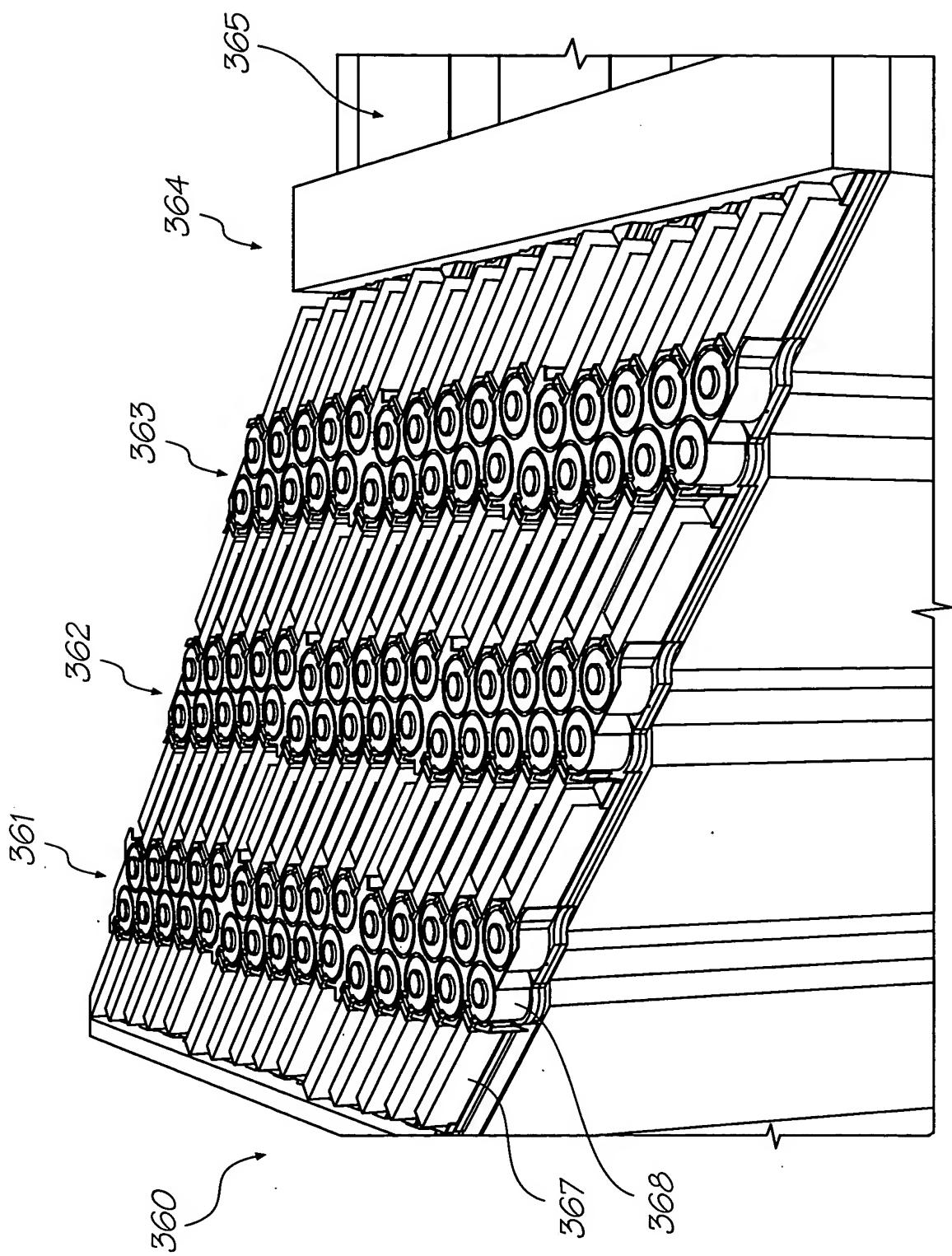


FIG. 85

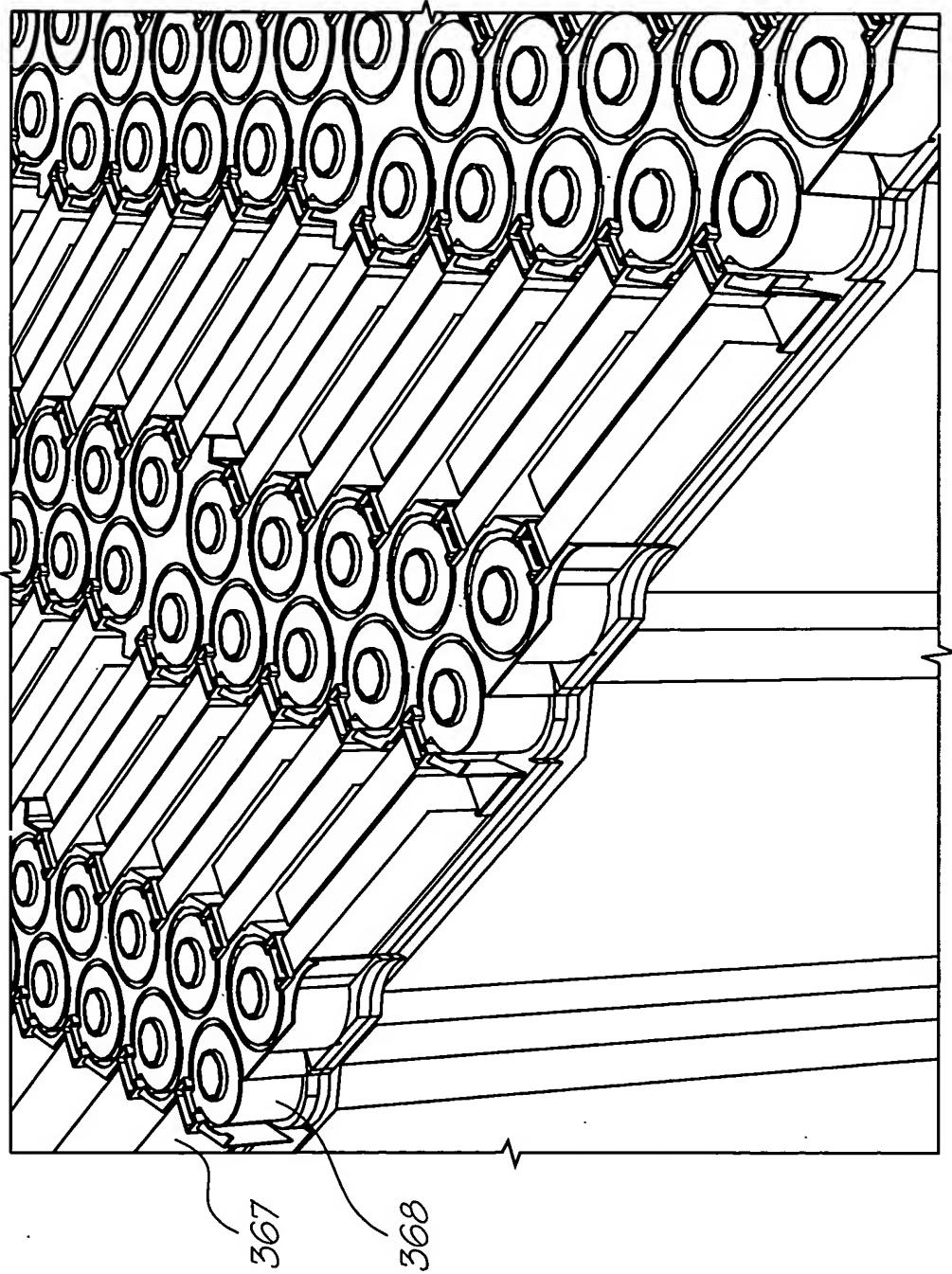


FIG. 86

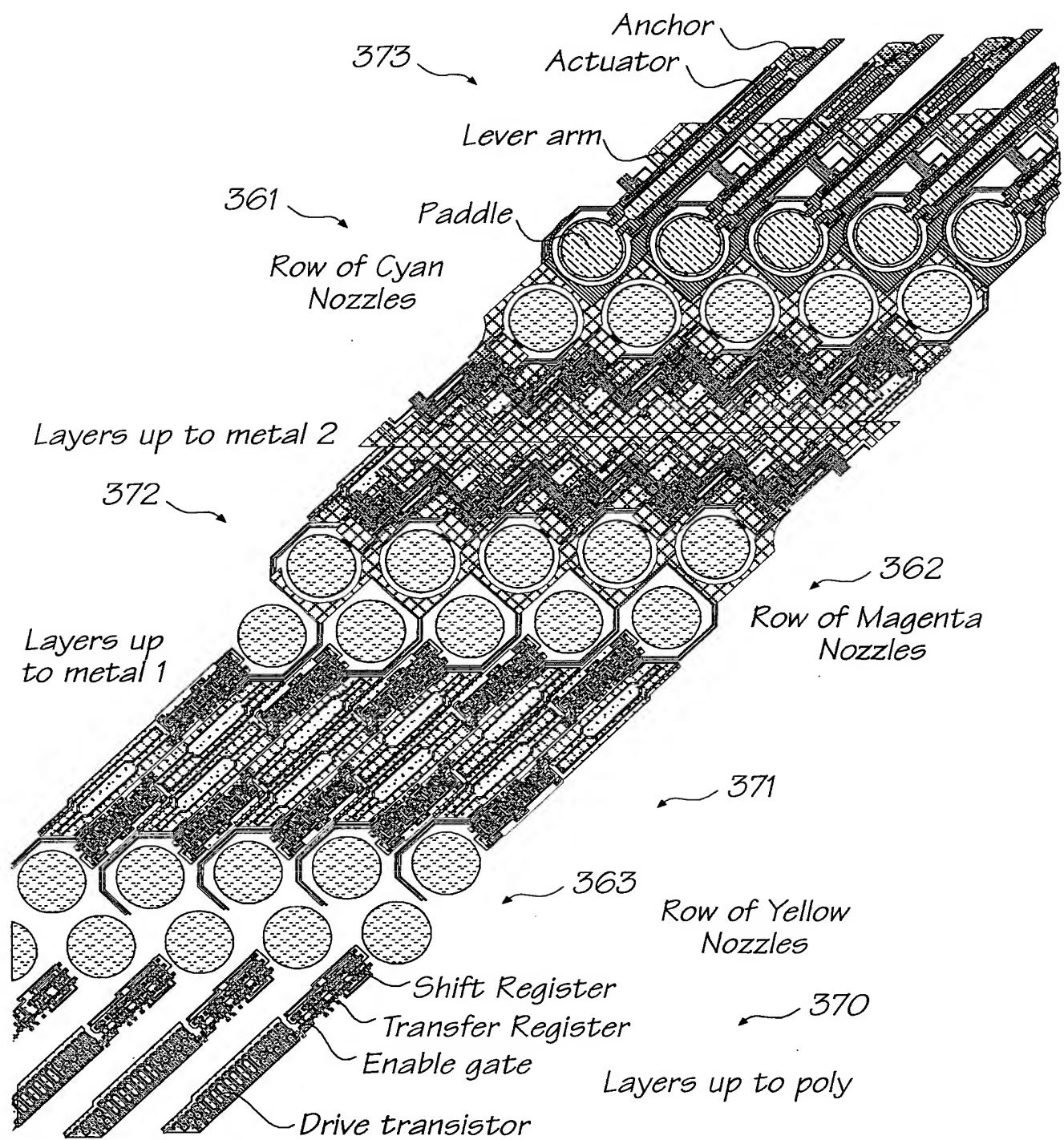


FIG. 87

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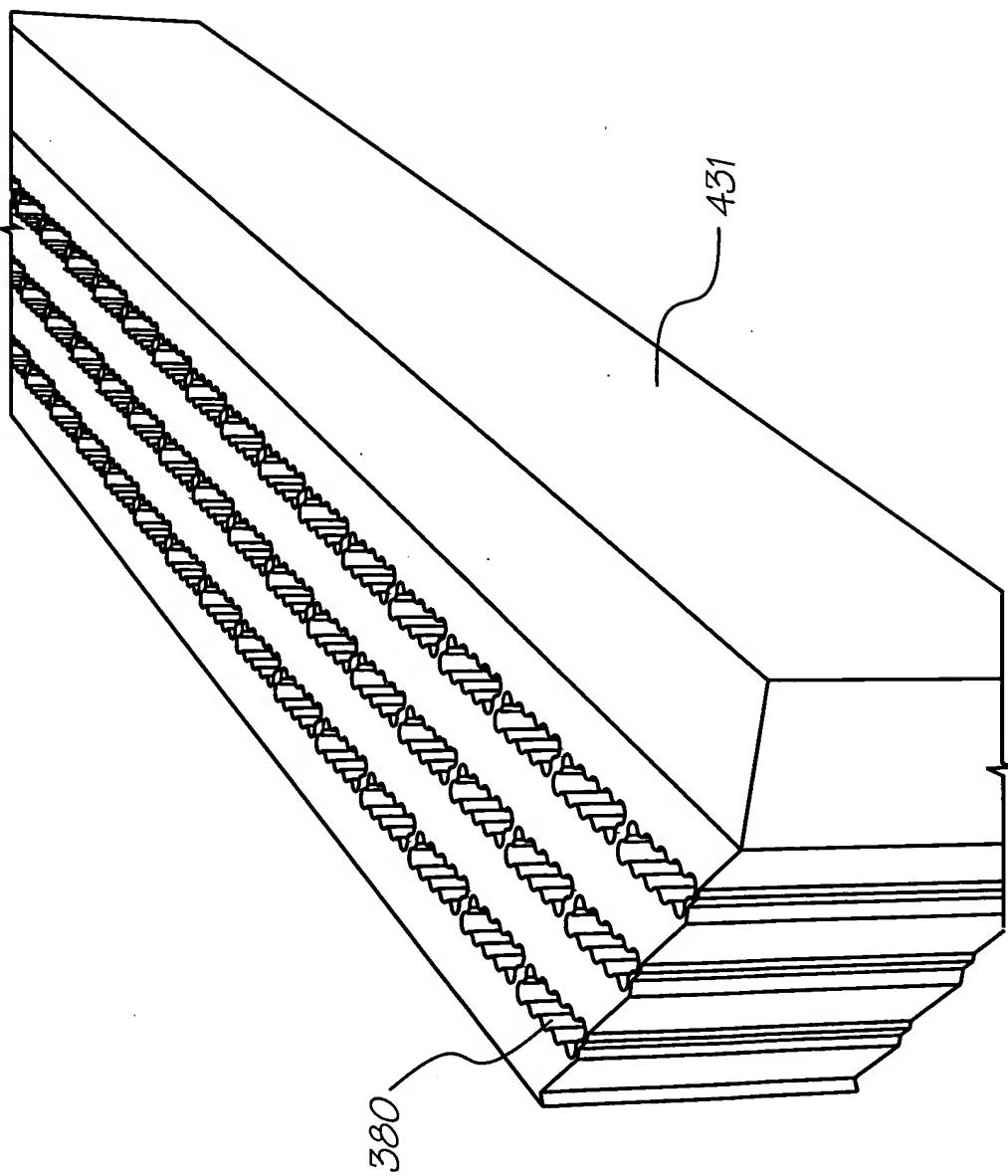


FIG. 88

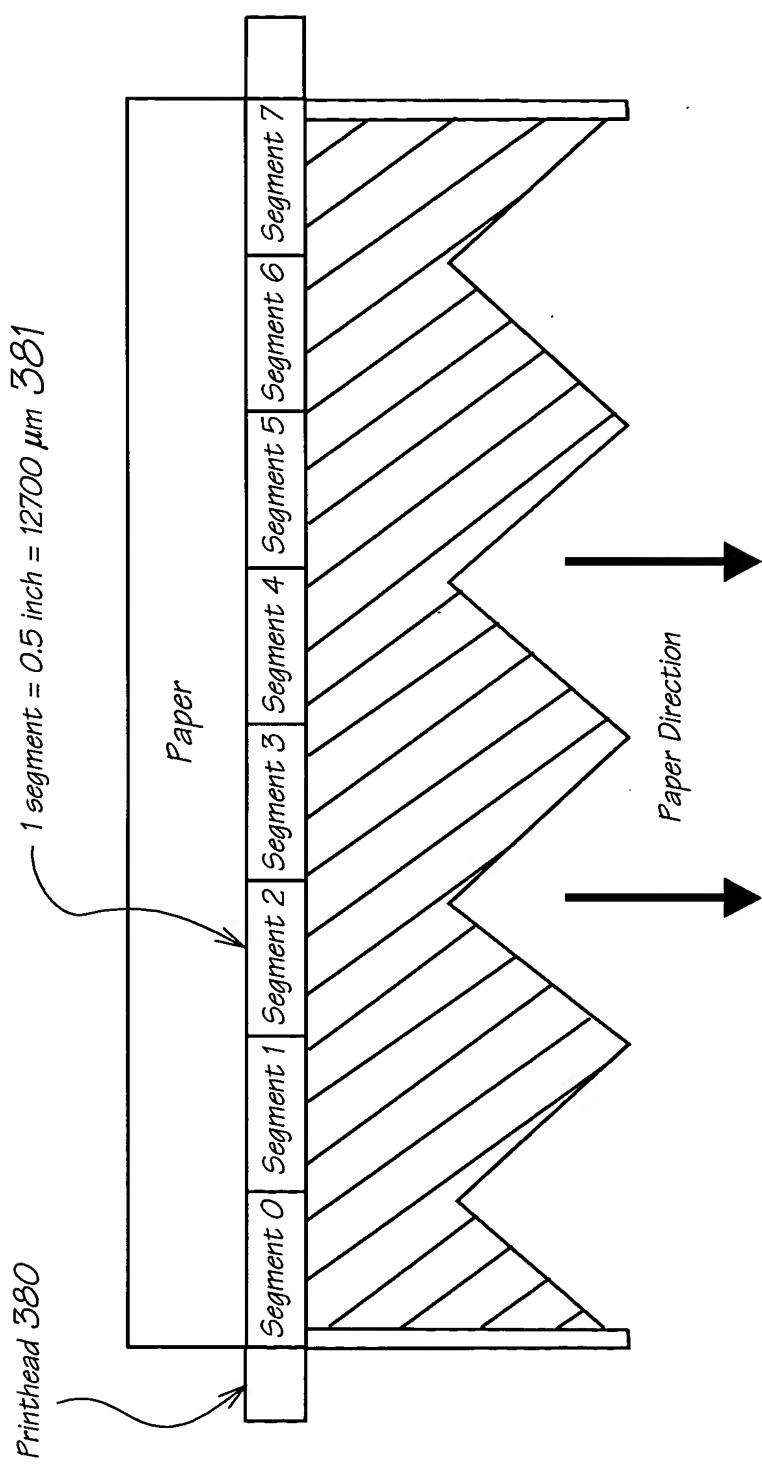
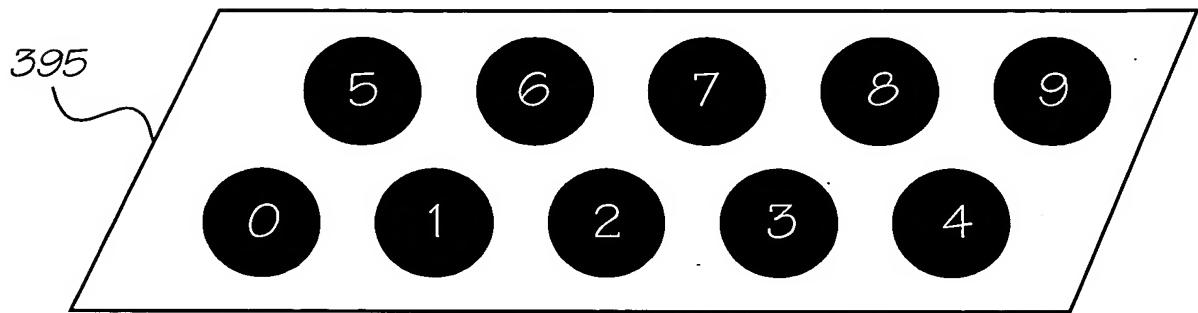
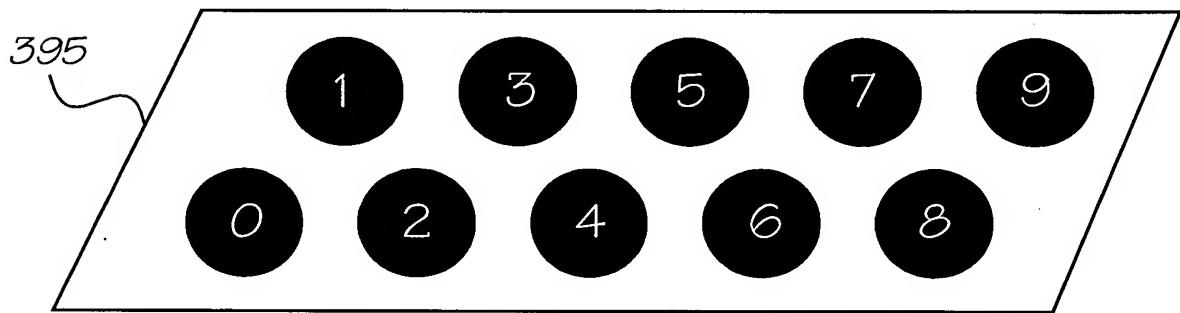


FIG. 89

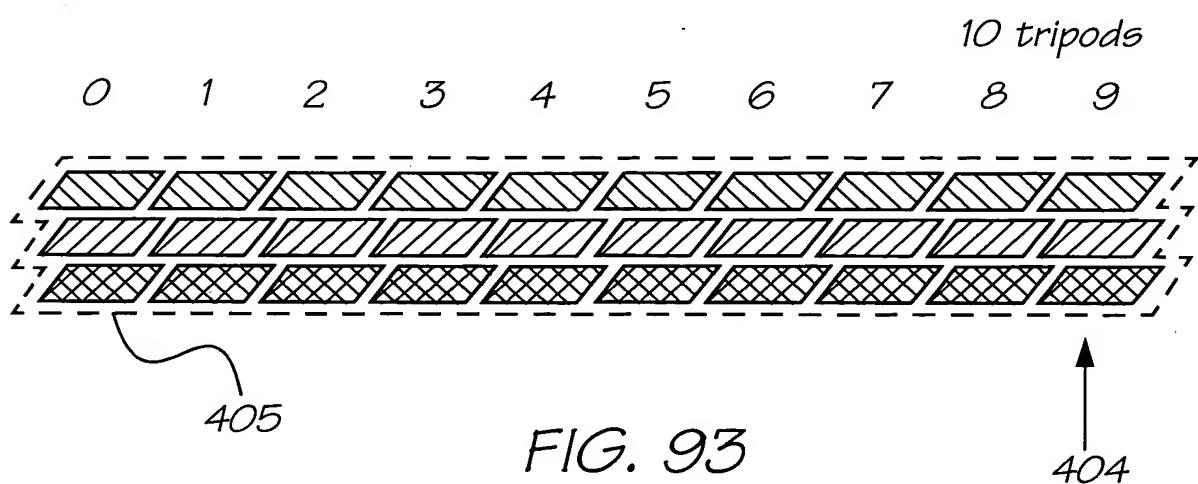


*A single pod, numbered by firing order*

*FIG. 90*



*FIG. 91*



*FIG. 93*

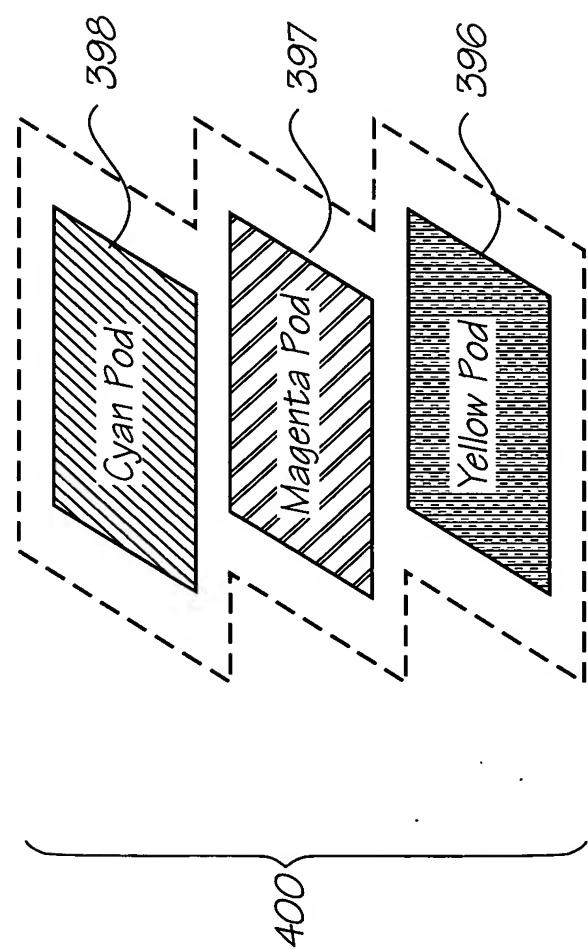


FIG. 92

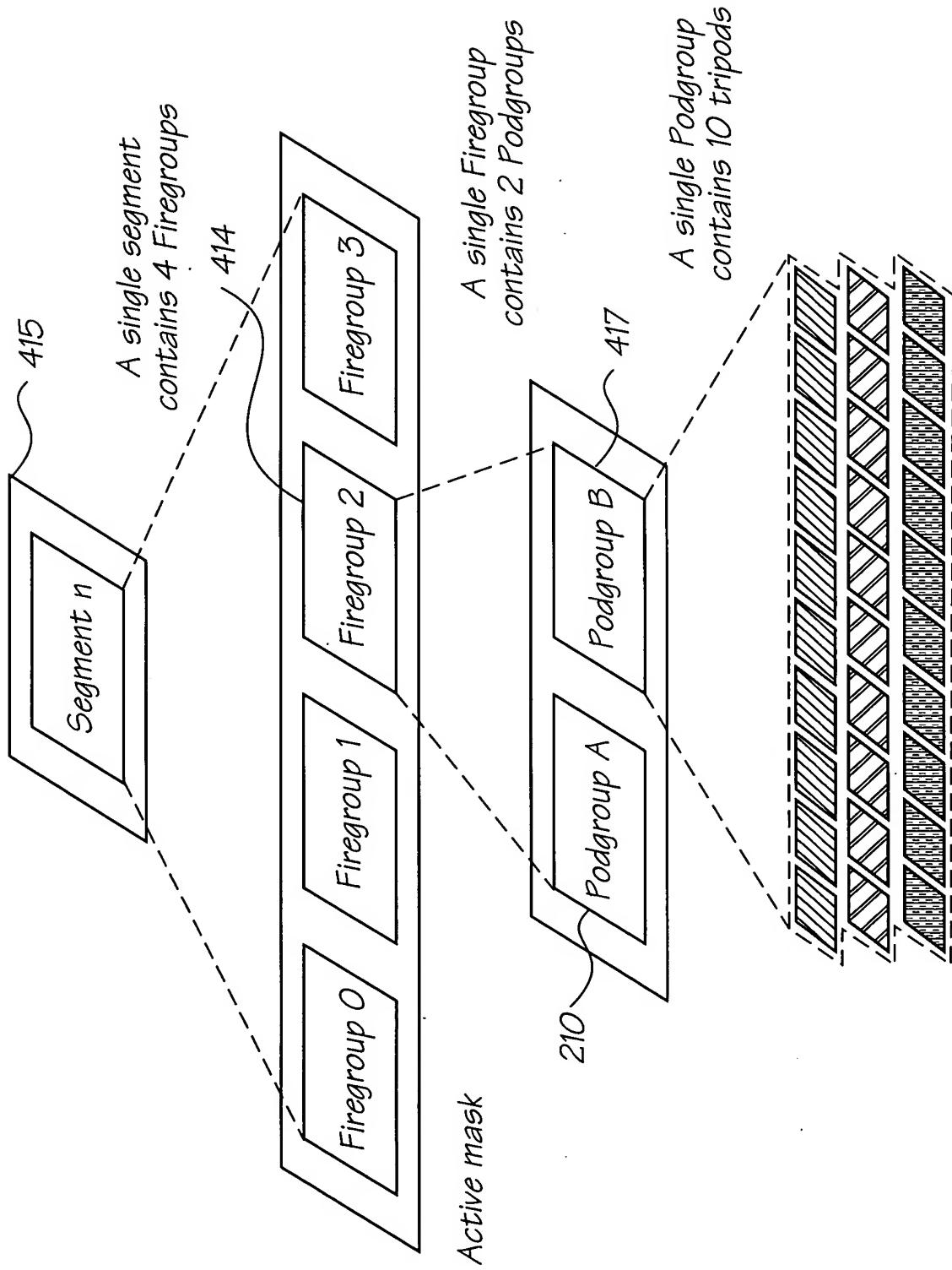


FIG. 94

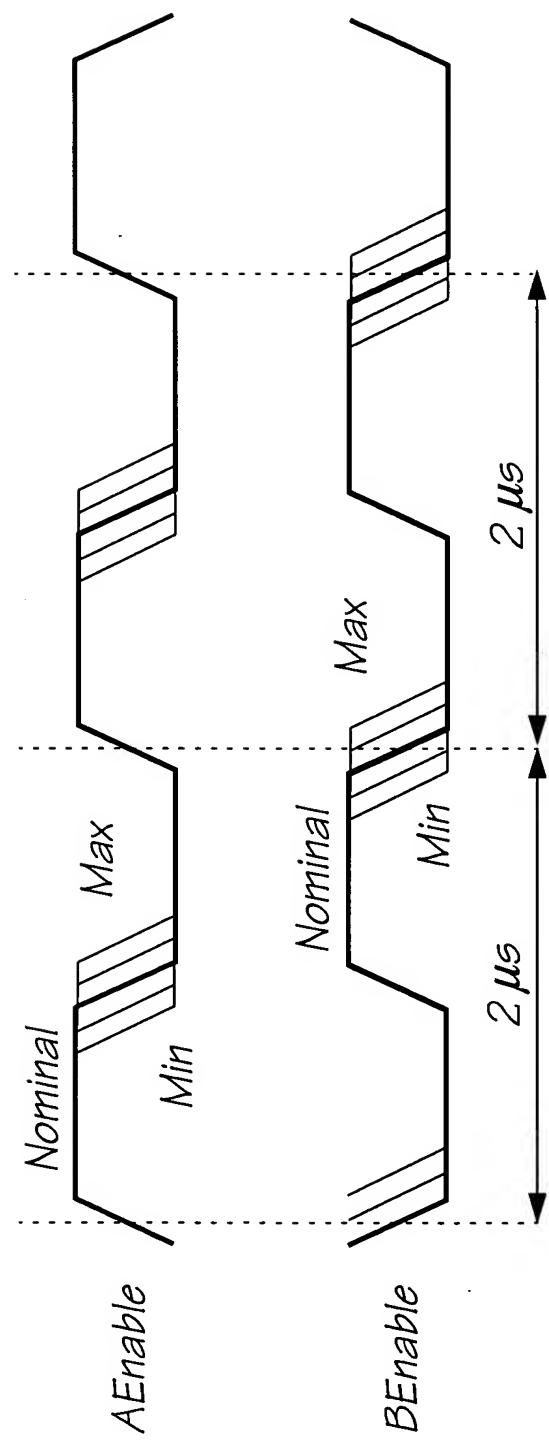


FIG. 95

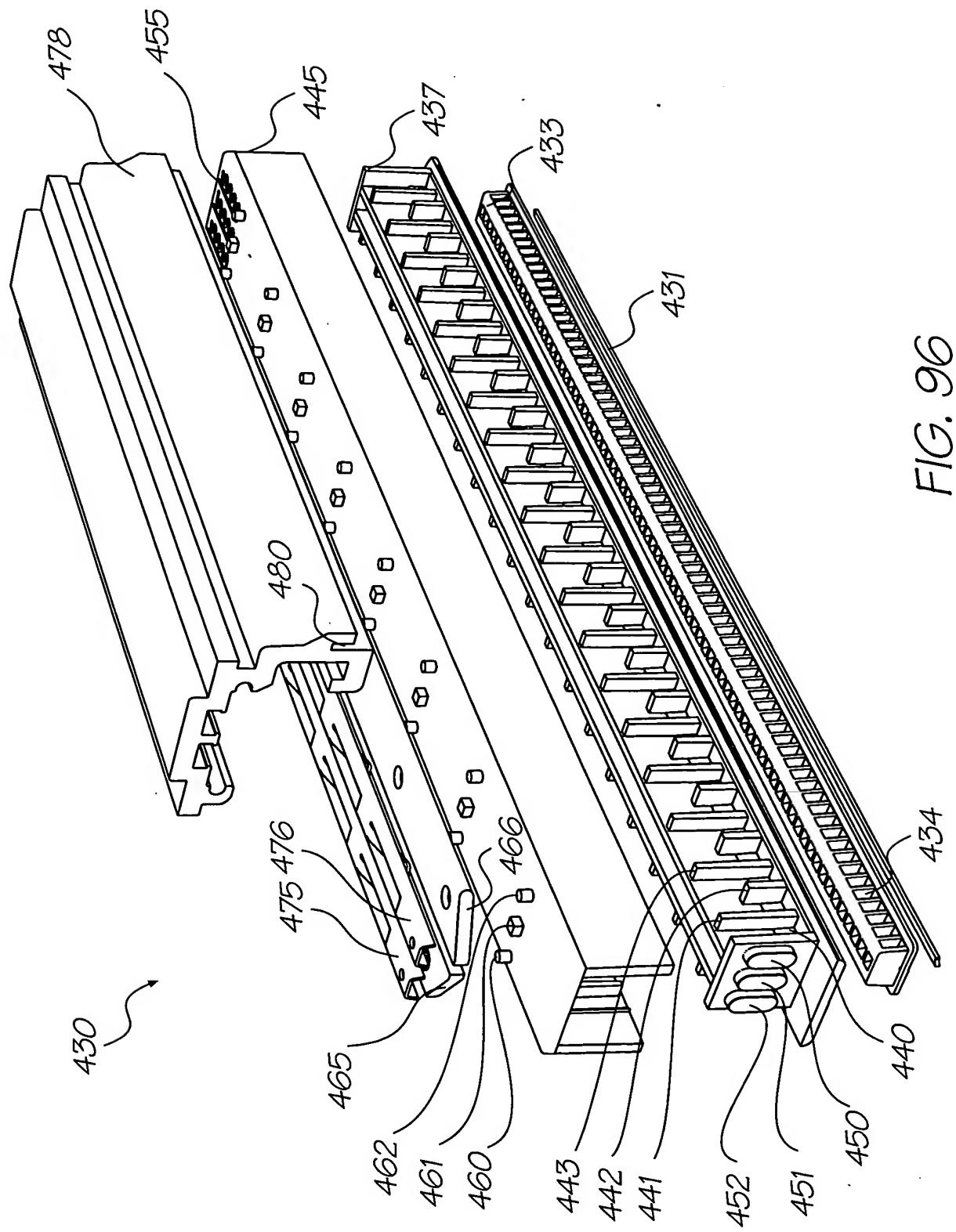


FIG. 96

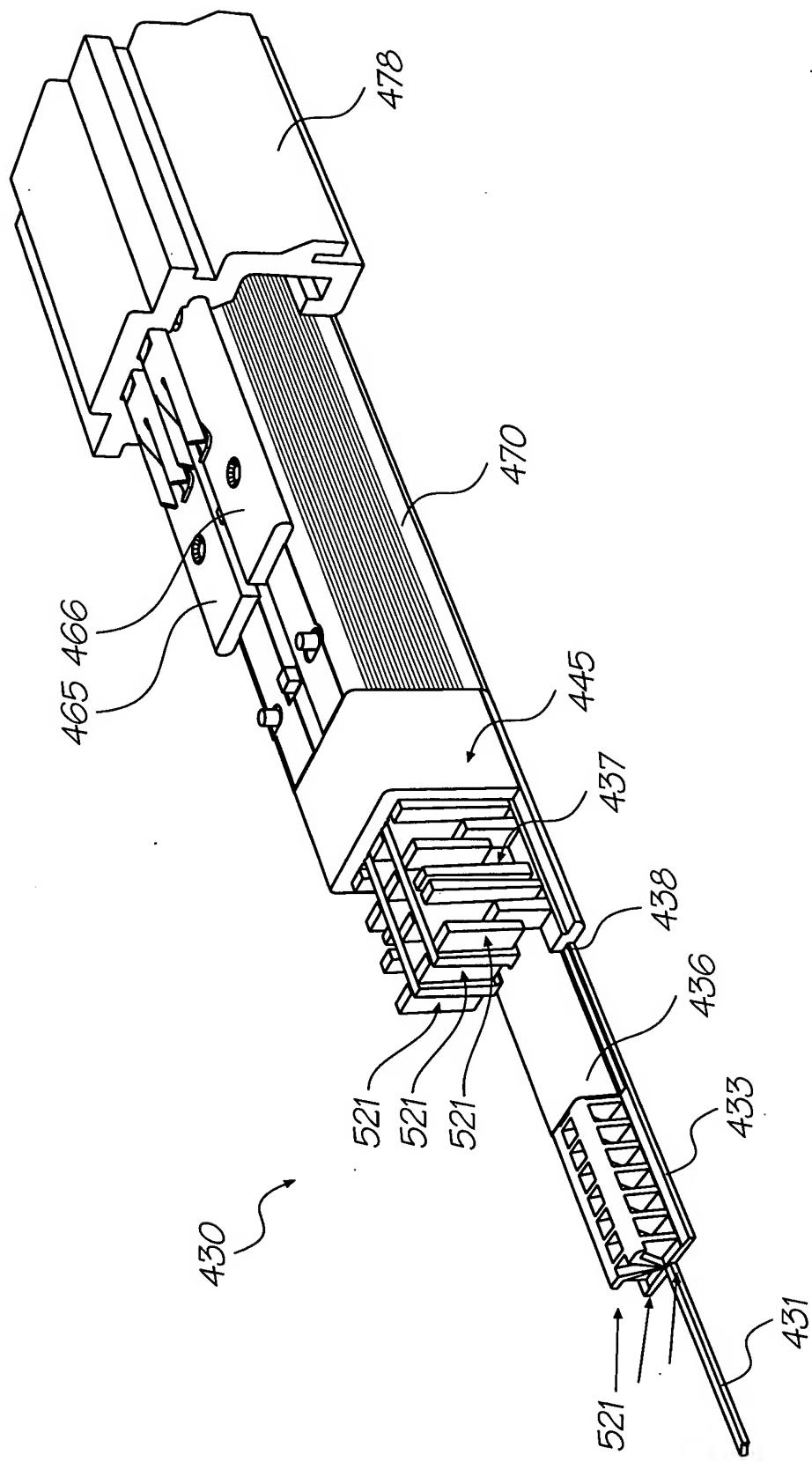


FIG. 97

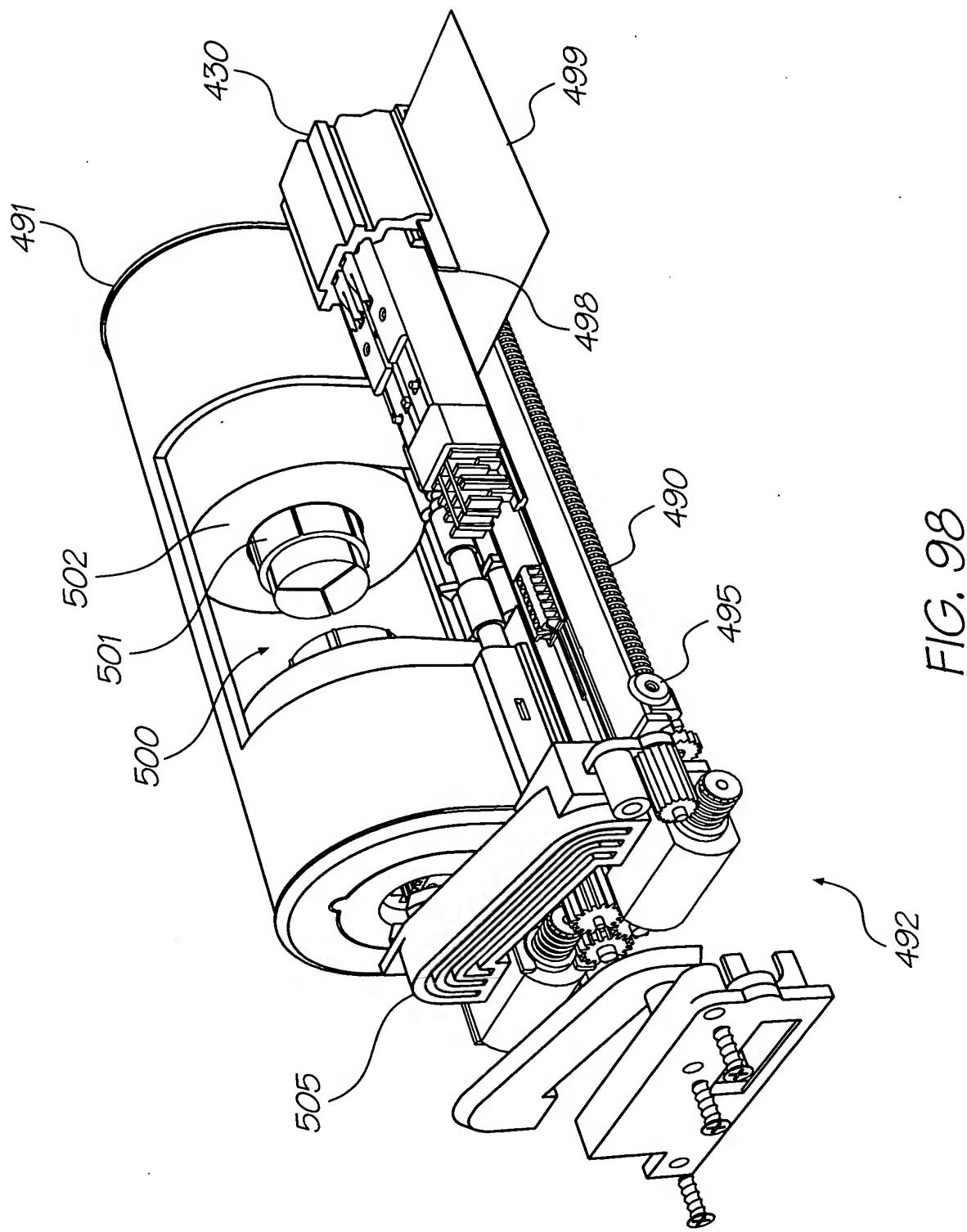


FIG. 98

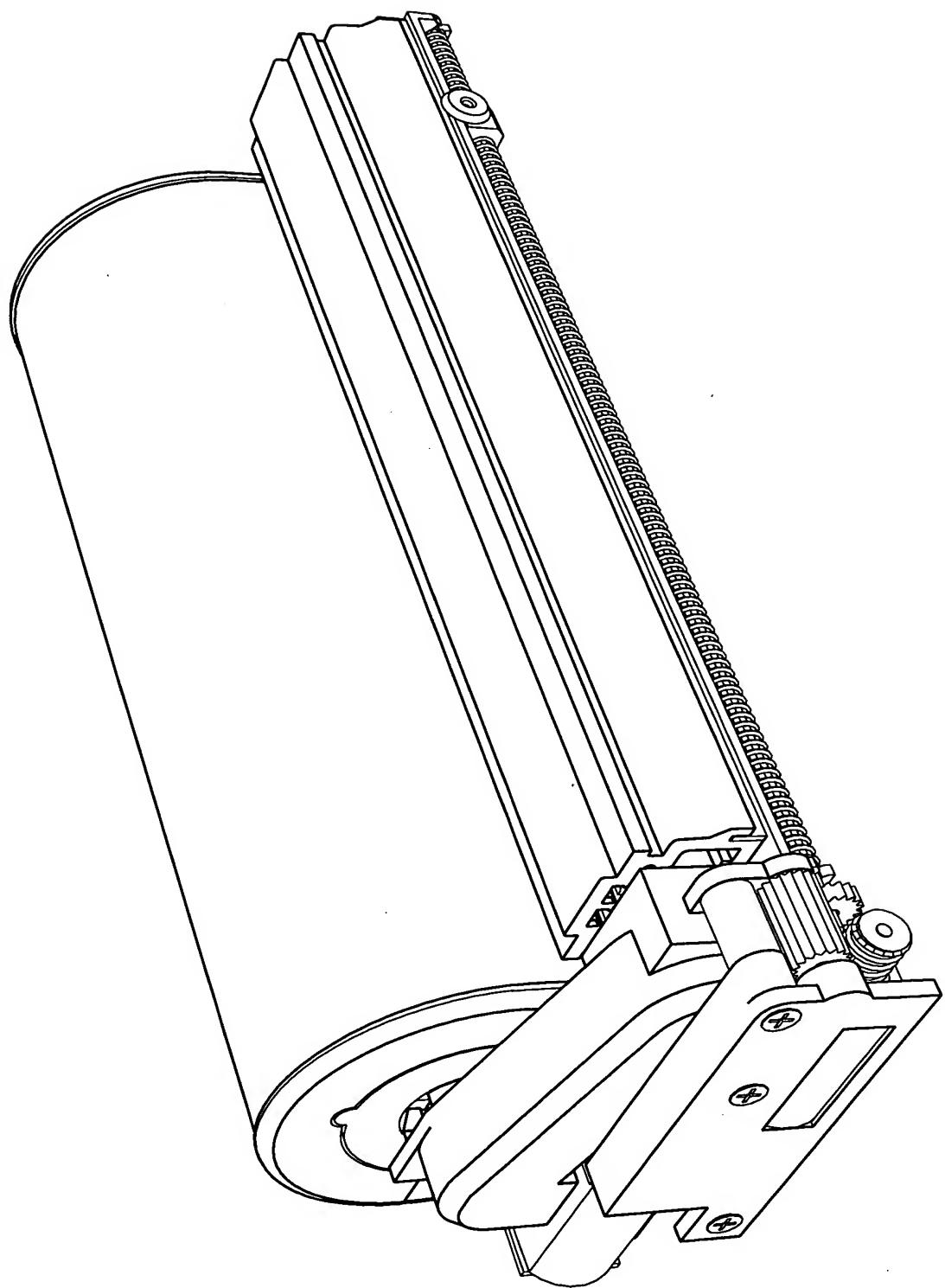


FIG. 99

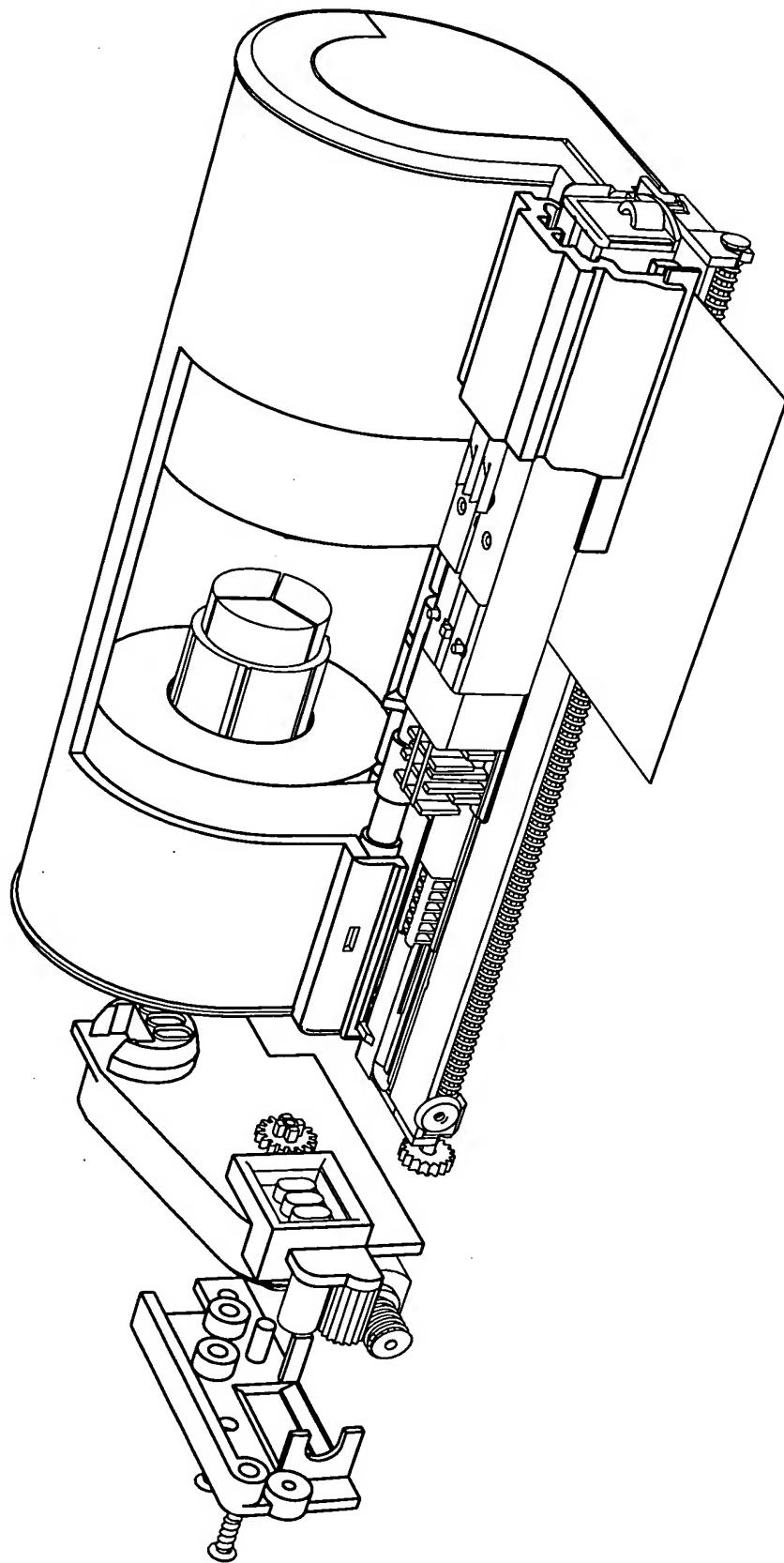


FIG. 100

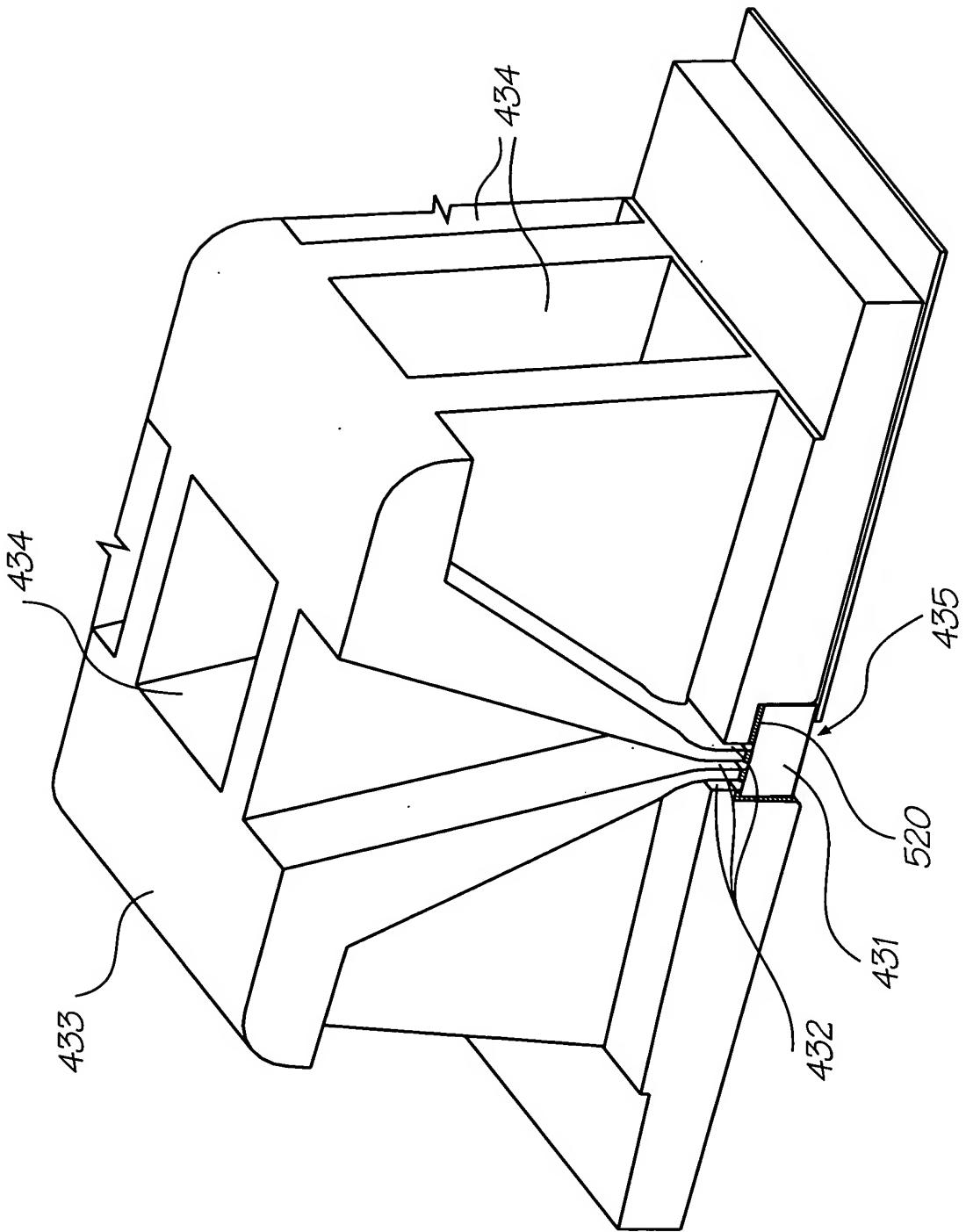


FIG. 101

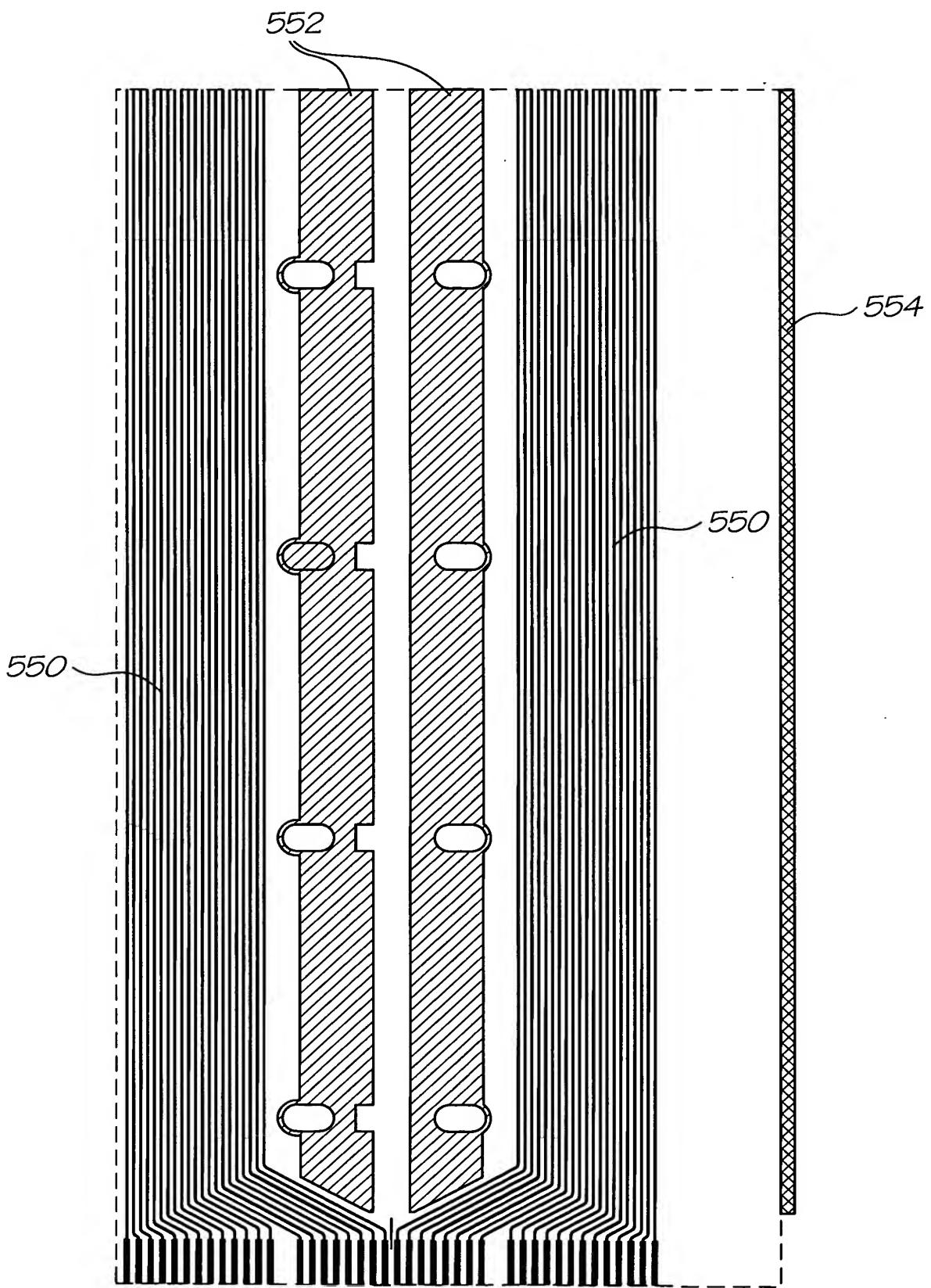


FIG. 102

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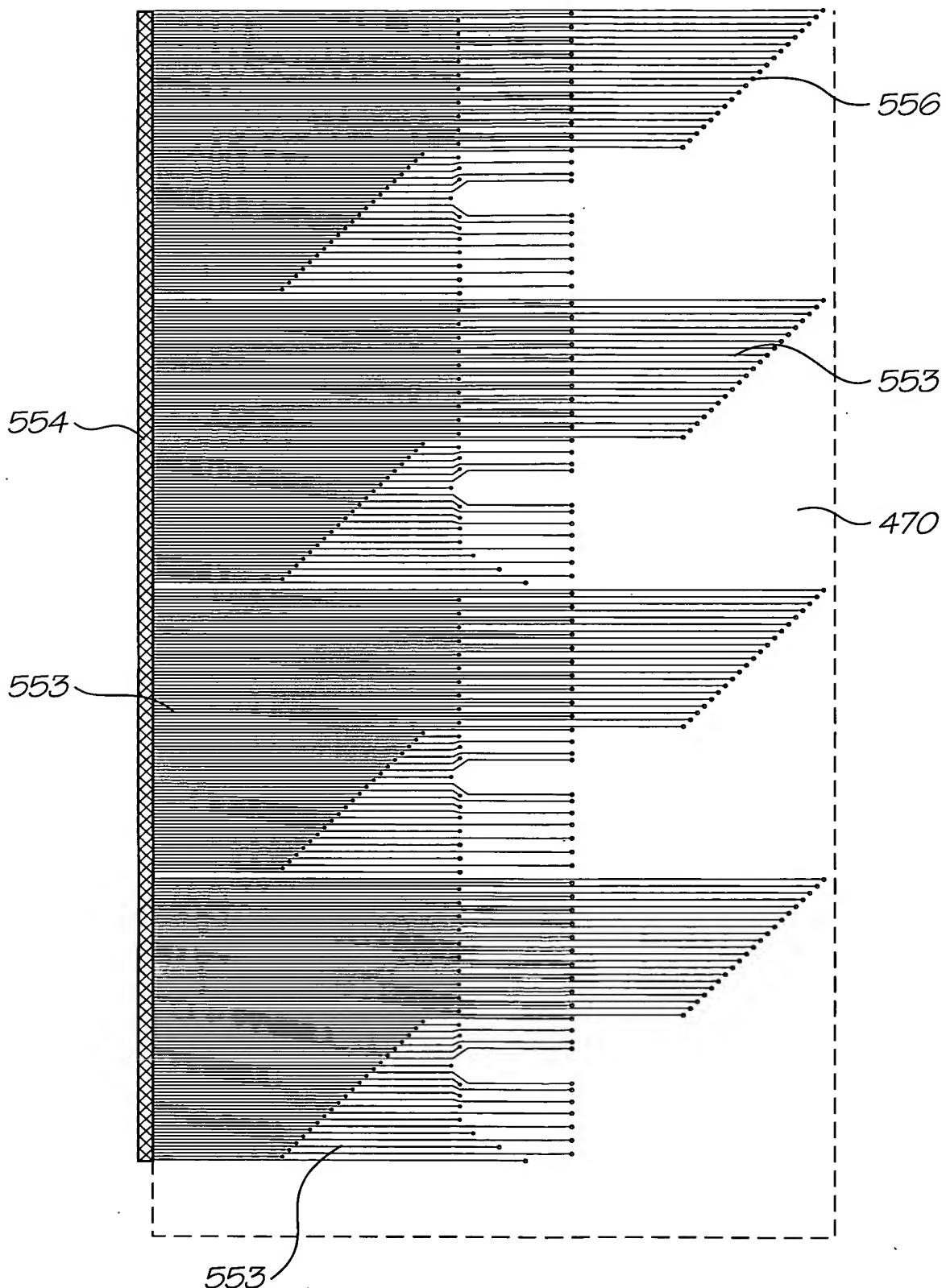


FIG. 103